Features

- Compliant with IEEE 802.11n, 11a, 11b, 11g
- Depopulated 73-pin lead-free/RoHS compliant
- WLCSP 4.10 mm x 3.84 mm x 0.6 mm with
- 0.4 mm pitch
- Single-band reference design using 15 external components including SMPS power management: 1 x front-end module with HB PA and antenna switches, 15 capacitors and one inductor in a footprint of <60 mm2
- Dual-band reference design using 18 external components including SMPS power management: 1 x front-end module with HB PA and antenna switches, 1 x balun, 16 capacitors and three inductor in a footprint of <70 mm2
- Enhanced integrated Bluetooth coexistence
  - ePTA: proprietary enhanced coexistence hardware and algorithms
- Power supply
  - Integrated SMPS for direct battery connection
  - Software adjustable output voltage to minimize power consumption
- Clocks
  - Reference clock input (digital or sine wave)
  - Low power clock input at 32.768 kHz
  - Direct external crystal input for reference clock
- Various on-chip auto calibration features
- Support for 6 Mbps to 65 Mbps OFDM, 11 Mbps and 5.5 Mbps CCK and legacy 2 Mbps and 1 Mbps DSSS data rates
- WLAN solution with fully integrated:
  - Zero IF (ZIF) transceiver
  - OFDM and CCK baseband processors
  - ARM9 Media Access Controller (MAC)
  - SPI serial host interface
  - SDIO (1-bit, 4-bit) serial host interface
- Wi-Fi Direct support with concurrent operation
- Intelligent power control, including 802.11 power save mode
- Supports MAC enhancements including:
  - 802.11d - Regulatory domain operation
  - 802.11e - QoS including WMM
  - 802.11h – Transmit power control dynamic and frequency selection
  - 802.11i - Security including WPA2 and
  - WAPI compliance
  - 802.11k - Radio resource measurement
  - 802.11r - Roaming
  - 802.11w - Management frame protection

Description

The ACC1340 is an IEEE 802.11a/b/g/n WLAN single-chip solution fully optimized applications such as video transmission, audio playback and IoT. The extremely low power consumption and intelligent host off loading of beacon as well as the packet processing ensure industry leading power savings. High levels of integration allow for very compact and cost effective reference designs delivering fast time-to-market for new WLAN enabled products.

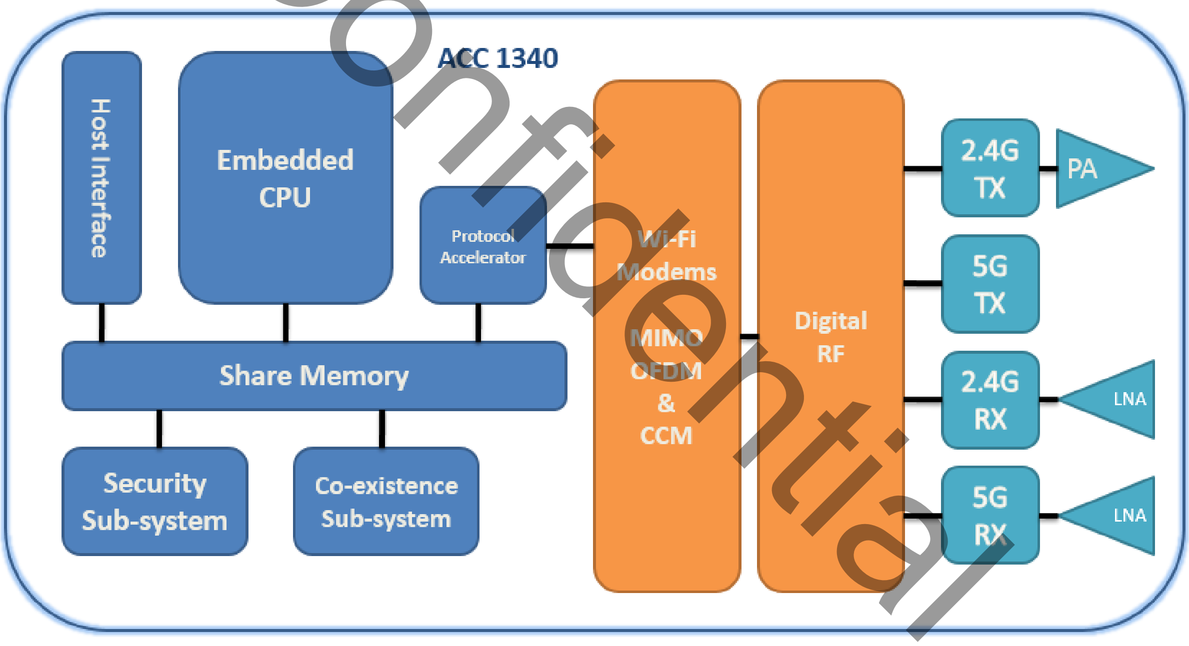
Contents

1. Introduction

The ACC1340 is an IEEE 802.11a/b/g/n WLAN single-chip solution fully optimized for mobile applications such as mobile phones, smart phones, PDAs, and portable media players. The extremely low power consumption and intelligent host off loading of beacon as well as the packet processing ensure industry leading battery life. High levels of integration enabling very compact and cost effective designs, delivering fast time-to-market for new WLAN enabled products, integrating a power amplifier and switch mode power supply. All ports are single ended, except for the 2.4 GHz TX port that is differential. The ACC1340 offers proprietary enhanced BT-WLAN coexistence, power consumption, shared power supply, and clock reducing WGBF BOM costs. A comprehensive suite of software is provided that includes proven drivers for Linux/Android along with production test and engineering software utilities.

The ACC1340 is a system-on-chip WLAN device packed in Wafer Level Chip Scale Package (WLCSP) of 4.10 mm x 3.84 mm x 0.6 mm with 0.4 mm pitch.

Figure 1. ACC1340 (simplified) block diagram



The ACC1340 SoC is built on the proven success of previous generation WLAN devices, providing the lowest power consumption, best-in-class BT- WLAN co-existence mechanism in addition to high throughput performance and better range. The ACC1340 supports a comprehensive range of 802.11 standards and amendments:

- Enhanced throughput and range through 802.11n support – single stream with support for Wi-Fi 802.11n certification including STBC RX and STBC control frame optional features
- 2.4 GHz and 5 GHz operation compliant to 802.11a/b/g
- QoS support compliant to 802.11e/WMM/WMM-PS standards
- Robust security based on 802.11i/WPA/WPA2 standards
- Regulatory domain operation support based on 802.11d operation
- Transmit power control and dynamic frequency selection support based on 802.11h standard
- Radio resource measurements support based on 802.11k standard
- Fast BSS transition support based on 802.11r standard
- Protected management frame support based on 802.11w standard
- Easy and secure setup support based on Wi-Fi protected setup standard
- Supports peer-to-peer communication based on Wi-Fi Direct
- Supports concurrent Wi-Fi and Wi-Fi Direct operation

The ACC1340 also supports Cisco® compatible extensions (CCX™ v2, v3, v4, and CCX™ Lite).

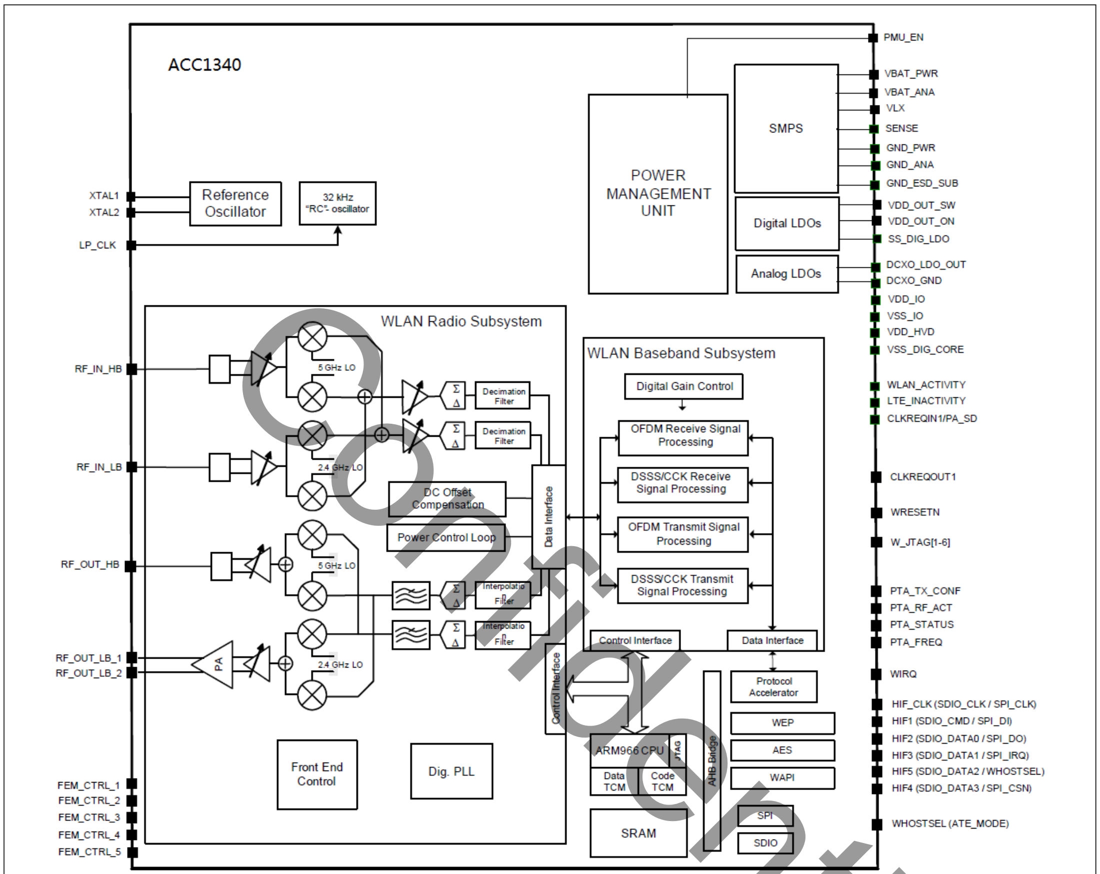
The WLAN subsystem includes a dual-band ZIF transceiver, RF synthesizer/VCO, high- speed data converters, an OFDM/CCK digital baseband processor, a power amplifier for the 2.4 GHz band, a switch mode power supply, and an ARM9-based MAC.

A comprehensive single band reference design is provided that includes a switch that combines the TX and RX ports from the WLAN with the RF port from a Bluetooth device onto one 2.4 GHz antenna. A band-pass filter is added between the switch and the antenna depending on the presence of other wireless devices in the same application. The dual- band reference design adds a Front-End Module (FEM) that includes the PA and the antenna switch for the 5 GHz WLAN band. Depending on the preferred implementation, the FEM can include the 2.4 GHz band switch and a diplexer can be added for a dual-band single antenna configuration.

2. General Hardware Description

2.1. Block Diagram

Figure 2. ACC1340 complete diagram



2.2. Electrical Data

2.2.1. Absolute maximum ratings

The Absolute Maximum Rating (AMR) corresponds to the maximum value that can be applied without leading to instantaneous or very short-term unrecoverable hard failure (destructive breakdown).

Table 1. Absolute maximum ratings

Symbol	Parameter	Min	Max	Unit
V_{BAT}	Direct battery connect supply voltage	-0.3	+5.5	V
V_{DD_HV}	Supply voltages	-0.3	+2.0	V
V_{DD_IO}	Supply voltage I/O	-0.3	+2.0	V
V_{in}	Input voltage on any digital pin	-0.3	+2.0	V
V_{ssdiff}	Maximum voltage difference between different types of Vss pins	-0.3	+0.3	V
T_{stg}	Storage temperature	-65	+150	°C

2.2.2. Operating ranges

Operating ranges define the limits for functional operation and parametric characteristics of the device. Functionality outside these limits is not guaranteed.

Table 2. Operating ranges

Symbol	Parameter	Min	Typ	Max	Unit
T_{amb}	Operating ambient temperature	-40	+25	+85	°C
V_{BAT}	Direct battery connect supply voltage: – All specs guaranteed – All specs guaranteed with output power back-off – Device functional with reduced performances	3.6 2.7 2.3	- - -	4.8 3.6 2.7	V V V
V_{DD_HVD}	Supply voltages – All specs guaranteed – Device functional with reduced performances	1.65 -	1.8 1.6	1.95 -	V V
V_{DD_IO}	I/O supply voltage 1.8 V mode	1.65	1.8	1.95	V
	I/O supply voltage 1.2 V mode	1.1	1.2	1.3	V

2.2.3. Digital I/O specifications

All I/Os, except analog I/Os or otherwise specified are standard I/Os with levels complying with the EIA/JEDEC standard JESD8-7.

Table 3. DC and AC input specifications

Symbol	Parameter	Min	Typ	Max	Unit
Input levels					
V_{IL}	Low-level input voltage	0	-	0.35 * V_{DD_IO}	V
V_{IH}	High-level input voltage	0.65 * V_{DD_IO}	-	-	V
V_{hyst}	Schmitt trigger hysteresis	150	-	-	mV
T_r/T_f	Rise and fall time that can be present on inputs	-	-	25	ns
R_i	Input resistance	1	-	-	MΩ
C_i	Input capacitance	-	-	5	pF
Output levels					
V_{OL}	Low-level output voltage (@ +100 µA)	0	-	0.2	V
V_{OH}	High-level output voltage (@ -100 µA)	V_{DD_IO} - 0.2	-	V_{DD_IO}	V
T_r/T_f	Rise and fall time that can be present on outputs at Cload = 20 pF max	-	-	10	ns

Table 4. Pull-up and pull-down characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
R_{PU}	Equivalent pull-up resistance	V_{DD_IO} = 0 V	-	50	-	kΩ
R_{PD}	Equivalent pull-down resistance	V_{DD_IO} = 1.8 V	-	50	-	kΩ

Table 5. IOL and IOH characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I_{OL}	Sink current	V_{OL} = Max	X(1)	-	-	mA
I_{OH}	Source current	V_{OH} = Min	X(1)	-	-	mA

1. X can be 2, 4, or 8 depending on the type of the I/O (X denotes the drive strength of output stage).

Note: If the V_{DD_IO} supply is powered down, the external activity on the IOs is not allowed.

2.2.4. Handling information

Inputs and outputs are protected against electrostatic discharges during handling and mounting. All pins withstand threshold voltages as given in the following table:

Table 6. ESD threshold voltages

Parameter	Method	Value	Class
ESD threshold voltage	HBM (JESD22-A114-F)	±1 kV(1)	Class Ic
	CDM (JESD22-C101-D)	±200 V(1)	Class II

1. The weakest pins are RF IN LB and RF IN HB.

2.2.5. Thermal characteristics

Table 7. Package thermal resistance

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Θ_{J-A}	Junction-to-air thermal resistance	Eight layers PWB construction Board dimensions = 76 x 102 x 1 mm Natural convection	33(1)	-	46(2)	°C/W
Ψ_{J-B}	Junction-to-board thermal resistance		20(1)	-	28(2)	°C/W

1. NVTTE V4 with top side heat spreader (50 x 50 x 1 mm)
2. NVTTE V2

2.2.6. Clock specifications

The ACC1340 uses two clocks: a reference clock and a low power clock. For the reference clock, the ACC1340 can either use an external reference clock source or generate its own reference using a XTAL and a built-in oscillator. The low-power clock must always be supplied from an external source.

Table 8. Reference clock overall specifications

Symbol	Paramete r	Min	Typ	Max	Unit
Using an external reference clock					
F_{IN}	Clock input frequency list	13, 16, 16.8, 19.2, 26, 33.6, 38.4, 40, 52			MHz
F_{INTOL}	Tolerance on input frequency	-20	-	+20	ppm
t_{STABLE}	Clock stabilization time(1)	-	<10	15(2)	ms
Using one XTAL and the built-in oscillator					
F_{IN}	Clock input frequency list	38.4, 40, 52			MHz
F_{INTOL}	Combined inaccuracies of the XTAL after tuning	-20	-	+20	ppm

1. Time between clock request signal asserted by the IC until reference clock is stable. It is recommended that the system provides a stable clock in less than 10 ms.
2. Software programmable waiting time up to maximum 15 ms by discrete steps.

Table 9. Low power clock specifications

Symbol	Parameter	Min	Typ	Max	Unit
F_{IN}	Clock input frequencies		32.768		kHz
F_{INTOL}	Tolerance on input frequency	-1000	-	+1000	ppm

2.2.7. Current consumption

Table 10. ACC1340 current consumption

State	V_{BAT} (inc PA)		V_{BAT} (exc PA)		V_{IO}		Unit
	Typ	Max	Typ	Max	Typ	Max	
T_{amb} = 25 °C, 26 MHz digital clock, V_{BAT} = 3.6 V, V_{DD_HV} = 1.8 V, V_{DD_IO} = 1.8 V.							
Complete power down (WRESETN low, PMU_EN high)	61	-	56	-	7	-	µA
Complete power down (WRESETN low, PMU_EN low)	10	-	5	-	7	-	µA
Sleep	80	-	75	-	25	-	µA
Power save (beacon period (including DTIM) 100 ms, beacon length 1 ms) - proprietary power saving features disabled - proprietary power saving features enabled	 1.02 0.85	 - -	 1.01 0.85	- - -	 0.06 0.03	 - -	 mA mA
RX (idle[1], 2.4 GHz)	72	-	72	-	0.07	-	mA
RX (active[2], 2.4 GHz, OFDM)	75	-	75	-	0.87	-	mA
TX (active[2], 2.4 GHz, OFDM) 17.0 dBm @ RF port[3] 20.8 dBm @ RF port[4] 20.5 dBm @ RF port[5]	 270 350 340	-	 112 112 112	-	 0.67 0.67 0.67	-	 mA mA mA
RX (idle, 5 GHz)	69	-	68	-	0.87	-	mA
RX (active[2], 5 GHz, OFDM)	79	-	76	-	0.67	-	mA
TX (active[2], 5 GHz, OFDM), 15.3 dBm @ RF port[3]	273	-	95	-	0.67	-	mA
TX (active[2], 5 GHz, OFDM), 19.3 dBm @ RF port[3]	295	-	95	-	0.67	-	mA
A VoIP call using a standard codec G.711 (64 Kb/s, 320 byte packets) and U-APSD (WMM power save) power-saving mode.	5.18	-	4.10	-	0.04	-	mA
Video streaming; the device is receiving 2.0 Mbps of data using legacy PSM mode (for example, MPEG-4 @ 2 Mbps)	15.03	-	13.16	-	0.06	-	mA
I_{peak}: system maximum peak current draw[6]	-	398	-	-	-	-	mA
T_{amb} = 25 °C, 26 MHz digital clock, V_{BAT} = 3.6 V, V_{DD_HV} = 1.6 V, V_{DD_IO} = 1.8 V							
Complete power down (WRESETN low, PMU_EN high)	60	-	55	-	7	-	µA
Complete power down (WRESETN low, PMU_EN low)	10	-	5	-	7	-	µA
Sleep	76	-	71	-	25	-	µA
Power save (beacon period (including DTIM) 100 ms, beacon length 1 ms) - proprietary power saving features disabled - proprietary power saving features enabled	 0.89 0.74	 - -	 0.88 0.74	 - -	 0.06 0.03	 - -	 mA mA
RX (idle[1], 2.4 GHz)	64	-	64	-	0.07	-	mA
RX (active[2], 2.4 GHz, OFDM)	67	-	67	-	0.87	-	mA
TX (active[2], 2.4 GHz, OFDM), 15.5 dBm @ RF port[3]	242	-	97	-	0.67	-	mA
TX (active[2], 2.4 GHz, OFDM), 20.5 dBm @ RF port[3]	338	-	97	-	0.67	-	mA

TX (active[2], 2.4 GHz, OFDM), 19.0 dBm @ RF port[3]	285	-	97	-	0.67	-	mA
A VoIP call using a standard codec G.711 (64 Kb/s, 320 byte packets) and U-APSD (WMM power save) power-saving mode.	4.61	-	3.54	-	0.04	-	mA

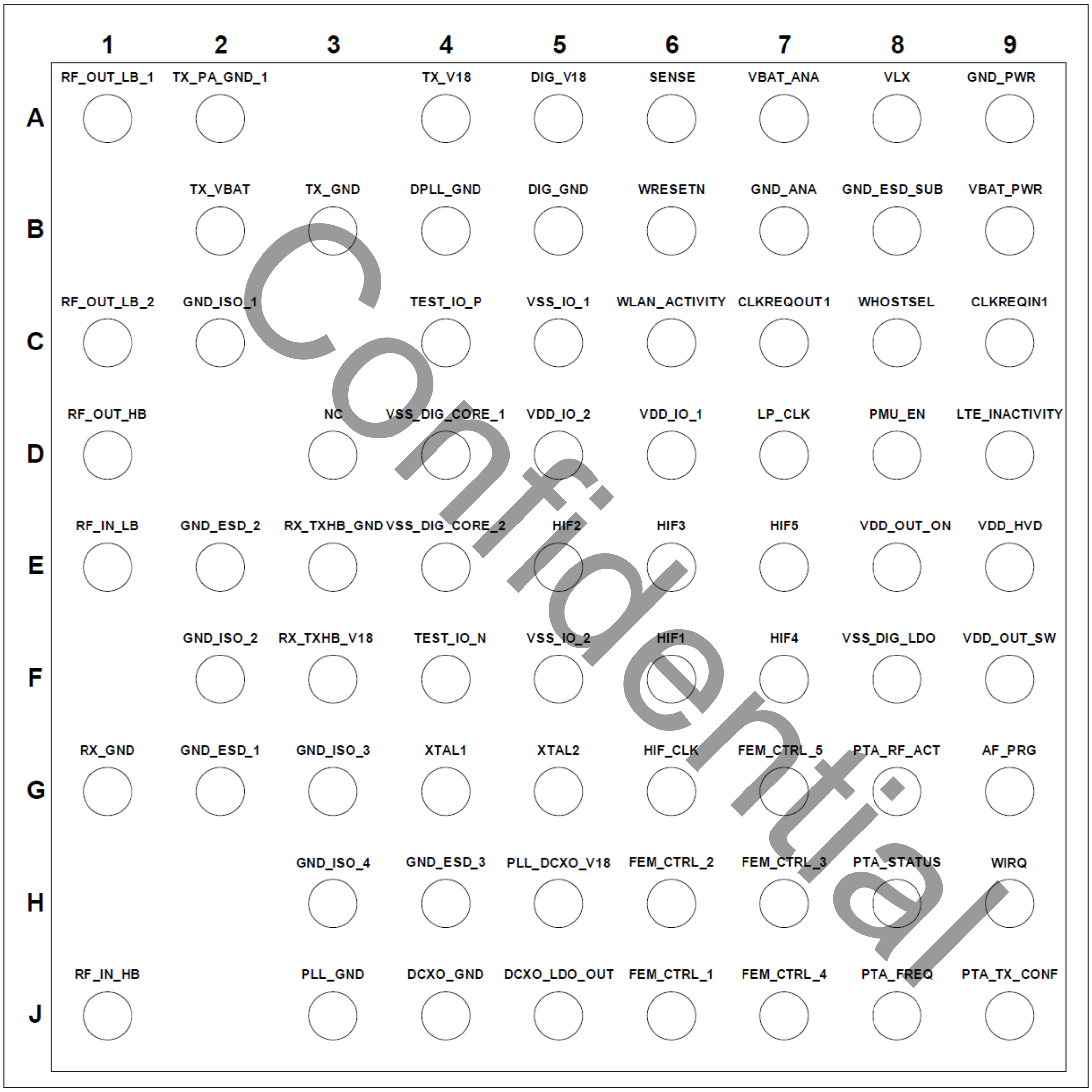
State	V_{BAT} (inc PA)		V_{BAT} (exc PA)		V_{IO}		Unit
	Typ	Max	Typ	Max	Typ	Max	
Video streaming; the device is receiving 2.0 Mbps of data using legacy PSM mode (for example, MPEG-4 @ 2 Mbps)	13.21	-	11.34	-	0.10	-	mA
I_{peak}: system maximum peak current draw[6]	-	378	-	-	-	-	mA

1. All RX circuitry is enabled but there is no signal to be received.
2. 100% of the time.
3. Typical Pout setting for 65 Mbps.
4. Typical Pout setting for 1 Mbps 11b mode, corresponding to 18 dBm@ANT.
5. Typical Pout setting for 6 Mbps.
6. Including all power rails of the ACC1340 connected directly or indirectly (through SMPS) to V_{BAT}. Excluding the additional draw from V_{BAT} due to other circuits supplied by the SMPS output.

2.3. Pinout

2.3.1. Pin layout

Figure 3. ACC1340 pinout top view



2.3.2. Pin functions

Table 11. ACC1340 functional and supply pin list

Name	Pin	Type	Reset		Description	Function during and after reset
			IO dir	Pull status		
Clock signals						
XTAL1	G4	I/O	I/O	None	Reference clock input or XTAL inputs	
XTAL2	G5	I/O	I/O	None		
LP_CLK	D7	I	I	None	Low power clock input	
Control signals						
WRESETN	B6	I	I	PD	Reset - active low	
WHOSTSEL	C8	I	I	None	Test mode selection - Active high	
CLKREQIN1	C9	I/O	I	PD	Programmable pin	CLKREQIN1/PA_SD
CLKREQOUT1	C7	I/O	I	PD		CLKREQOUT
WLAN_ACTIVITY	C6	I/O	O	drive LOW		WLAN_ACTIVITY
PMU_EN	D8	I/O	I	None (1)		SMPS enable(2)
LTE_INACTIVITY	D9	I/O	I	PD		LTE_INACTIVITY
Digital interfaces						
HIF1	F6	I/O	I	None	Programmable pin	SDIO_CMD/SPI_DI
HIF2	E5	I/O	I	None		SDIO_DATA0/SPI_DO
HIF3	E6	I/O	I	None		SDIO_DATA1/WIRQ
HIF4	F7	I/O	I	None		SDIO_DATA3/SPI_CSN
HIF5	E7	I/O	I	None		SDIO_DATA2/HIF selection(3)
HIF_CLK	G6	I/O	I	None		SDIO_CLK/SPI_CLK
PTA_TX_CONF	J9	I/O	I	PD		PTA_TXCONF
PTA_RF_ACT	G8	I/O	I	PD		PTA_RF_ACT(4)
PTA_STATUS	H8	I/O	I	PD		PTA_STATUS
PTA_FREQ	J8	I/O	I	PD		PTA_FREQ
WIRQ	H9	I/O	I	None		WIRQ
RF interfaces						
RF_IN_HB	J1	I (RF)	-	None	RX 5 GHz input	-
RF_IN_LB	E1	I (RF)	-	None	RX 2.4 GHz inputs	-
RF_OUT_HB	D1	O (RF)	-	None	TX 5 GHz output	-
RF_OUT_LB_1	A1	O (RF)	-	None	TX 2.4 GHz output	-
RF_OUT_LB_2	C1	O (RF)	-	None	TX 2.4 GHz output	-

Name	Pin	Type	Reset		Description	Function during and after reset
			IO dir	Pull status		
FEM control interfaces						
FEM_CTRL_1	J6	O	I	PD	Programmable pin	FEM controls
FEM_CTRL_2	H6	O	I	PD		
FEM_CTRL_3	H7	O	I	PD		
FEM_CTRL_4	J7	O	I	PD		
FEM_CTRL_5	G7	O	I	None		Bluetooth FEM control[5]
RF power supplies						
PLL_DCXO_V18	H5	-	-	-	1.8 V DCXO supply pin	
TX_V18	A4	-	-	-	1.8 V supply for WLAN RF transmit	
RX_TXHB_V18	F3	-	-	-	1.8 V supply	
TX_VBAT	B2	-	-	-	Supply for analog integrated PA (3.6 V)	
DIG_V18	A5	-	-	-	Supply for WLAN RF digital LDOs (1.8 V)	
DCXO_LDO_OUT	J5	-	-	-	Internal supply decoupling/regulator output	
GND_ESD_1	G2	-	-	-	Ground for WLAN analog	
GND_ESD_2	E2	-	-	-		
GND_ESD_3	H4	-	-	-		
DCXO_GND	J4	-	-	-		
GND_ISO_1	C2	-	-	-		
GND_ISO_2	F2	-	-	-		
GND_ISO_3	G3	-	-	-		
GND_ISO_4	H3	-	-	-		
TX_GND	B3	-	-	-	Ground for WLAN RF	
RX_GND	G1	-	-	-		
RX_TXHB_GND	E3	-	-	-		
TX_PA_GND_1	A2	-	-	-		
DIG_GND	B5	-	-	-	Ground for WLAN RF digital	
DPLL_GND	B4	-	-	-		
PLL_GND	J3	-	-	-	Ground for WLAN PLL	
Digital power supplies						
$V_{DD\_IO\_1}$	D6	-	-	-	Supply for digital I/Os (1.8 V)	
$V_{DD\_IO\_2}$	D5	-	-	-		
V_{DD_HVD}	E9	-	-	-	Supply for WLAN digital LDOs (1.8 V)	
$V_{DD\_OUT\_SW}$	F9	-	-	-	Internal supply decoupling/regulator output (1.2 V)	
VDD_OUT_ON	E8	-	-	-	Internal supply decoupling/regulator output (1.2 V)	

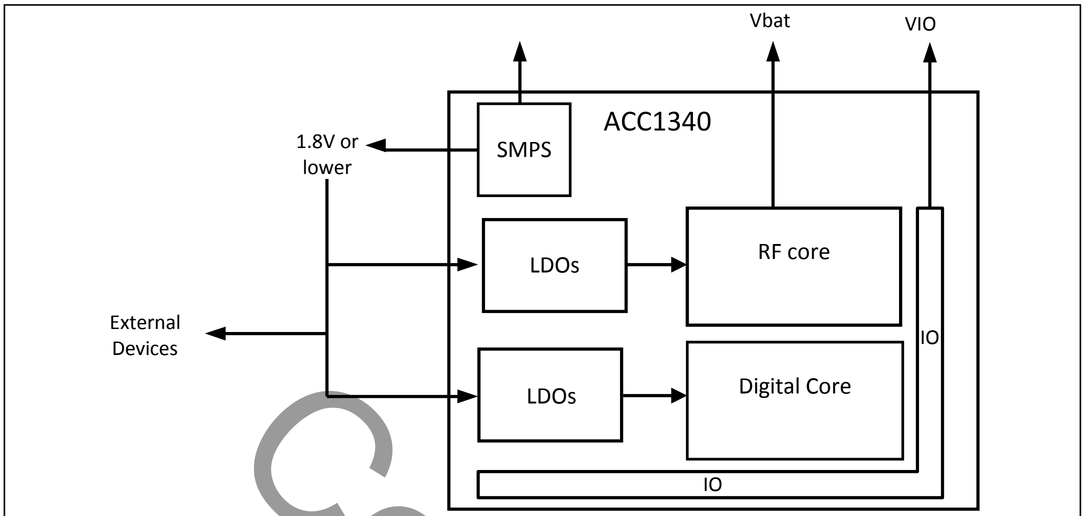
Name	Pin	Type	Reset		Description	Function during and after reset
			IO dir	Pull status		
VSS_IO_1	C5	-	-	-	Ground for digital	
VSS_IO_2	F5	-	-	-		
VSS_DIG_LDO	F8	-	-	-		
VSS_DIG_CORE_1	D4	-	-	-		
VSS_DIG_CORE_2	E4	-	-	-		
Other pins						
AF_PRG	G9	-	-	-	High voltage pad for antifuse programming (leave unconnected)	
TEST_IO_P	C4	-	-	-	WLAN ANA Test I/O (connected to VSS_W_ANA)	
TEST_IO_N	F4	-	-	-		
NC	D3	-	-	-	Not connected	
SMPS						
V_{BAT_PWR}	B9	-	-	-	Power stage supply pin	
V_{BAT_ANA}	A7	-	-	-	Analog supply pin	
GND_PWR	A9	-	-	-	Power stage ground pin	
GND_ANA	B7	-	-	-	Analog ground	
GND_ESD_SUB	B8	-	-	-	ESD substrate ground	
SENSE	A6	-	-	-	Voltage sense across external capacitor	
VLX	A8	-	-	-	Pin for inductor connection (switch output)	
No ball						
No ball	A3, B1, C3, D2, F1, H1, H2, J2	-	I/O	-	Those places in the grid are intentionally not occupied by any ball.	

1. Input with PD when external SMPS used (V_{BAT_PWR} and V_{BAT_ANA} connected to GND). Input without pull when internal SMPS used (V_{BAT_PWR} and V_{BAT_ANA} connected to V_{BAT}).
2. PMU_EN maintains some functionality when the ACC1340 is reset.
3. See *General control signals* for the host interface mode selection mechanism.
4. PTA_RF_ACT maintains some functionality when the ACC1340 is reset.
5. FEM_CTRL_5 maintains some functionality when the ACC1340 is reset.

2.4. Power supply

All circuits inside the ACC1340 but the IOs are supplied by a single battery connection. The IOs are supplied by a regulated 1.8 V source assumed to be available from the platform and on which the consumption does not exceed a few mA.

Figure 4. Simplified supply distribution architecture



2.4.1. SMPS

Features

- Two switching modes are supported:
  - PWM mode optimizes efficiency while minimizing ripple and noise for large current outputs
  - PFM mode optimizes efficiency for small current outputs
- Two output voltage configurations are supported:
  - 1.8 V to support the ACC1340 in combination with other components
  - A SW-programmable voltage between 1.8 V and 1.4 V that minimizes the ACC1340 consumption. This second case can be used when no other component requires 1.8 V from the built-in SMPS.
- Optionally disable the SMPS to use an external SMPS. This requires V_{BAT_PWR} and V_{BAT_ANA} to be tied to ground.
- High switching frequency allows the use of a small inductor value (hence a compact footprint) while maintaining a very low ripple at the output

SMPS use cases

Table 12. SMPS use cases

Use case	Configuration	Description
1	V_{BAT_PWR} and V_{BAT_ANA} connected to GND(1)	An external SMPS is used to supply the ACC1340. The built-in SMPS is disabled.

2	V_{BAT_PWR} and V_{BAT_ANA} connected to battery	The built-in SMPS is enabled. The selection of the output voltage is done in SW, taking into account the state of PMU_EN. For optimum operation, strap to GND. The SMPS will automatically switch from PWM to PFM depending on the current draw.

1. It is a good practice to connect both to GND.

SMPS control signals

Table 13. SMPS control signals

Signal	Use case	Direction	Function
PMU_EN	1	Output	PMU_EN indicates the WLAN transceiver's power request. Active high. Leave this pin unconnected if not used in this use case.
	2	Input	PMU_EN enables the SMPS. PMU_EN is internally combined (OR) with the WLAN transceiver power request. The circuitry behind PMU_EN is supplied by $V_{DD\_IO\_x}$. It remains functional when the WLAN transceiver is reset (WRESETN = low) or when its core is not supplied. Multiple request can be combined externally by a wired-OR. Active high.

PMU_EN should never be HIGH while VIO1 and VIO2 switch from HIGH to LOW.

SMPS other signals

Table 14. SMPS other signals

Signal	Direction	Function
V_{BAT_PWR}	Supply	Power stage supply pin. Electrical path to decoupling should be kept minimal. Connect this pin to GND in use case 1.
V_{BAT_ANA}	Supply	Analog supply pin. Connect this pin to GND in use case 1.
GND_PWR	GND	Power stage GND pin. Electrical path to decoupling should be kept minimal.
GND_ANA	GND	Analog GND pin.
GND_ESD_SUB	GND	ESD substrate GND pin.
SENSE	Input	It senses the voltage across the output capacitor. Leave unconnected or connect to GND in use case 1.
VLX	Output	SMPS output to be routed directly to the external LC. Leave unconnected or connect to GND in use case 1.

Figure 5. Use case 1: External SMPS application

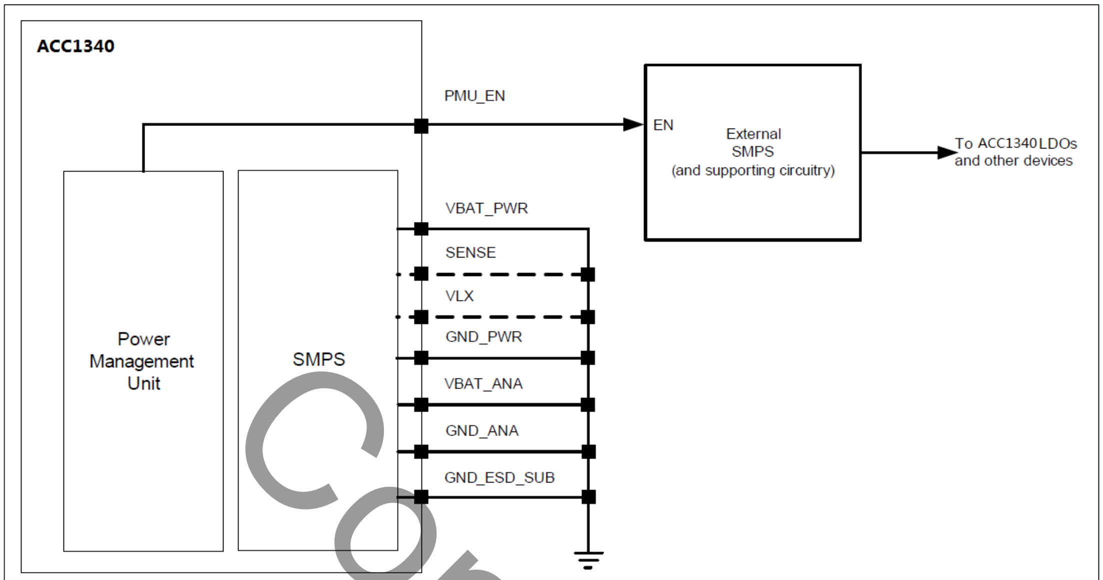


Figure 6. Use case 2: Internal SMPS application

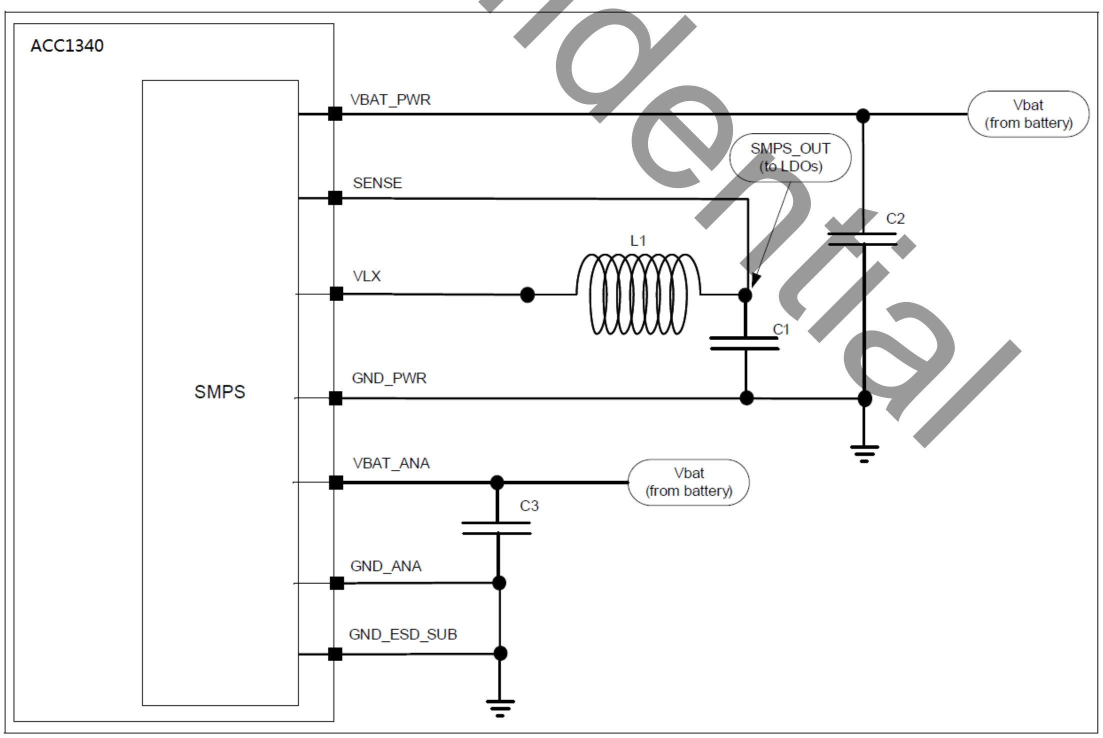
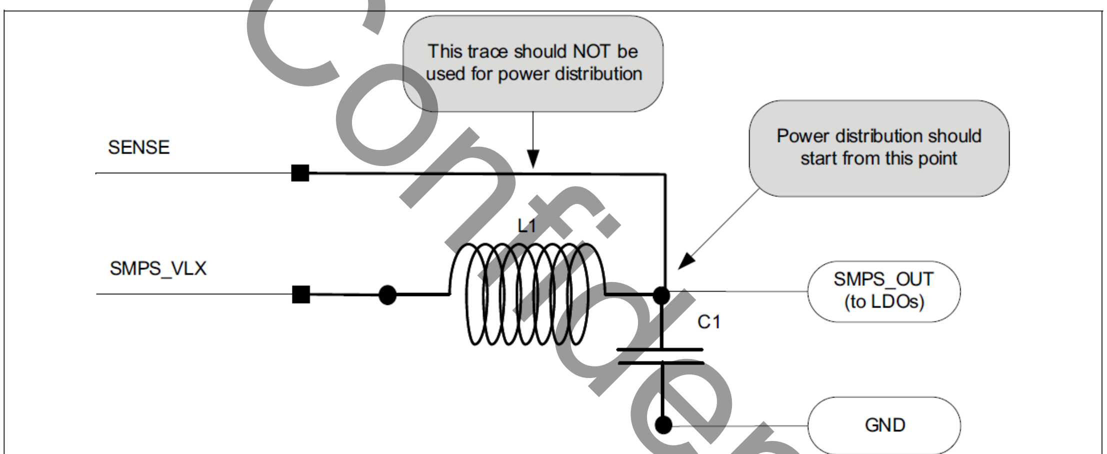


Table 15. Components for ACC1340 internal SMPS application

Component reference	Requirements	Suggested parts
L1	L = 1 µH I sat > 750 mA Rs < 200 mΩ	0603: Murata LQM18PN1R0NF0 0603: TDK GLCR1608T1R0M 0805: Murata LQM21PN1R0MC0
C1	C = 4.7 µF Rated voltage > 2.5 V Rs < 200 mΩ Ls < 0.750 pH	0402: Murata GRM155R60G475M / GRM155R60J475M
C2	C = 2.2 µF (or higher) Rated voltage ≥ 6.0 V Ls < 200 pH	0402: GRM155F50J225Z / GRM155R61A225K
C3	C = 100 nF Rated voltage ≥ 6.0 V	0201: GRM0336R0J104K

Figure 7 Precaution in the layout of the SMPS external components



SMPS performances

Table 16. SMPS performances

Specification	Conditions	Min	Typ	Max	Unit
Input voltage					
See operating ranges table					
Output voltage					
Vout (output high)	±5% accuracy	1.71	1.8	1.89	V
Vout (output low)	±5% accuracy	Programmable in SW			
Vout ripple (output high)(1)	PWM	-	-	10	mVpp
	PFM	-	-	40	mVpp
Vout load regulation	From 10% to 90% of Iload max or vice versa	-50	-	+50	mVpp
Vout line regulation	Input voltage drops 400 mv during GSM PA bursts	-50	-	+50	mVpp
Currents					
Ileak		-	1	-	µA
Iload max	Maximum peak current through L1 before hitting overload protection	675	750	825	mA

Table 16. SMPS performances (continued)

Specification	Conditions	Min	Typ	Max	Unit
Switching					
Fswitch	PWM switching frequency range. SW programmable	9	10	11	MHz
Efficiency and mode of operation					
Efficiency	PFM	80	-	-	%
	PWM	85	-	-	%
Iswitch	PFM if Iout ≤ Iswitch PWM if Iout > Iswitch	-	70	-	mA

1. The actual ripple on the supplied components is lowered by the presence of additional decoupling capacitors.

2.4.2. Power-up and power-down

Reset and power-up

There is no constraint on the power supplies (V_{DD_HV} and V_{DD_IO}) activation sequence. The device can start up without the reference clock being present. The device shall request it using one of the CLKREQOUTx signals. The platform is than expected to provide a stable clock within *Tstable* ms unless the built-in XTAL oscillator is used.

A valid reset shall be obtained by maintaining WRESETN active (low) for at least two cycles of LP_CLK after V_{DD_IO} is stable within its operating range. There is no constraint on the activation of the other supplies during this process. The reset is propagated to the core during the startup sequence described below.

A typical startup for the WLAN system is as follows:

1. VDD_IO is applied.
2. LP_CLK (low power clock) is running and stable.
3. The WRESETN pin is released after at least two LP_CLK cycles.
4. In case the internal SMPS is not used, PMU_EN is asserted. In case the internal SMPS is used, it is started. In both cases, VDD_HV gets a valid supply within 20 ms.
5. The host should wait 30 ms after the WRESETN release for the on-chip LDO to stabilize.
6. The device is now in the Sleep state.
7. The host should now wake the device by writing over the host interface, SPI or SDIO, to the WUP bit.
8. The device asserts CLKREQOUTx to request the reference clock.
9. Within Tstable ms, the reference clock should be stable and the system can start using it.
10. The device will set the RDY (ready) bit and assert IRQ to the host.
11. The host can download the firmware and release the CPU reset by further SPI/SDIO writes
12. The host now waits for the ACC1340 sub-system to initialize and can clear the WUP bit.
13. Once initialized, which includes a series of messages passing between the host and the WLAN, the WLAN may not have anything further to do and will enter the sleep state.

More detailed information on this startup sequence and the required host commands can be found in the hardware user manual.

To power down the device, PMU_EN and WRESETN have to be set to 0. SMPS will power down and its 1.8 V output will be pulled to 0 V. There are no constraints on other input pins (although it is recommended to give at least two LP_CLK cycles after asserting WRESETN = 0). V_{DDIO} is allowed to go down 20 ms after all input signals have been set to 0.

2.5. Clocks

2.5.1. Reference clock (system clock)

The reference clock is the main clock of the ACC1340. It is provided to the device either as a digital square wave input, a sinusoidal low amplitude signal, or is generated using a crystal directly connected to the device.

Table 17. Reference clock overall specifications

Symbol	Parameter	Min	Typ	Max	Unit
F_{IN}	Clock input frequency list Using an external clock source	13, 16, 16.8, 19.2, 26, 33.6, 38.4, 40, 52			MHz
	Clock input frequency list Using a XTAL and the built-in oscillator	38.4, 40, 52			MHz
F_{INTOL}	Tolerance on input frequency without trimming	-20	-	+20	ppm
$F_{INTTRIM}$	Tolerance on input frequency with trimming(1)	-50	-	+50	ppm
Tstable	Clock stabilization time(2)	-	< 10	15(3)	ms
I_{LEAK}	Input leakage current, both for analog and digital	-	-	1	µA

1. This is the initial acceptable range. Variation over time will however meet the FINTOL requirements.

2. Time from the moment the clock request signal is asserted by the IC until the reference clock is stable. It is recommended that the system provides a stable clock in less than 10 ms.

3. Wait for the software programmable time up to a maximum of 15 ms by discrete steps.

Clock frequency detection

An integrated automatic detection algorithm detects the reference clock frequency using the low power clock after a hardware reset.

Clock source detection

An integrated automatic detection mechanism detects the clock source from the connections of the XTAL1 and XTAL2 pins:

- When an external reference clock source is used, the clock input pin is XTAL2. The ACC1340 supports both an analog and digital source. An analog source shall be AC coupled to XTAL2 while a digital source shall be DC coupled to XTAL2. In both cases, XTAL1 shall be DC grounded.
- When a XTAL and the built-in oscillator are used, the XTAL shall be DC coupled to XTAL1 and XTAL2.

External clock source

Table 18. External clock requirements

Symbol	Parameter	Min	Typ	Max	Unit
AC coupled analog signal					
F_{in}	External clock frequency list	-	13, 16, 16.8, 19.2, 26, 33.6, 38.4, 40, 52	-	MHz
V_{APP}	Peak-to-peak voltage range of the AC coupled analog input	0.4	0.5	1.2	Vpp
N_H	Total harmonic content of the input signal	-	-	-25	dBc
DC coupled digital signal					
V_{IL}	ACC1340 input low voltage on XTAL1 and XTAL2(1)	0	-	0.3 * V_{DD_IO}	V
V_{IH}	ACC1340 input high voltage on XTAL1 and XTAL2(1)	0.7 * V_{DD_IO}	-	V_{DD_IO}	V
T_r/T_f	10%-90% rise and fall time	-	-	5	ns
Duty cycle		35	50	65	%
Both analog and digital signals					
Z_{INRe}	Real part of parallel AC input impedance at the pin	30	100	-	kΩ
Z_{INIm}	Imaginary part of parallel AC input impedance at the pin	-	2	4.7	pF
Z_{IDRe}	Change in real part of parallel impedance at the pin when changing mode(2) (expressed in equivalent parallel resistance added or removed)	150	-	-	kΩ
Z_{IDIm}	Change in imaginary part of parallel impedance at the pin when changing	-	-	0.5	pF
Z_{DC}	DC input impedance	10	-	-	MΩ
$Jitter_{cc}$	Cycle-to-cycle jitter, 6 sigma value	-	-	250	ps
$Jitter_{pp}$	Peak-to-peak jitter during clock activation to ensure that PLL stays locked	-	-	1	ns
Phase noise	Ref clock @ 26 MHz, 2.4 GHz 802.11b/g/n operation @1 kHz @10 kHz @100 kHz @1 MHz	-	-	-123 -133 -138 -138	dBc/Hz
	Ref clock @ 26 MHz, 5 GHz 802.11a/n operation @1 KHz @10 kHz @100 kHz @1 MHz	-	-	-127.5 -140.5 -144 -144.5	dBc/Hz

1. Those are not the same as the V_{IH} and V_{IL} of other digital IOs.
2. When changing from a mode where the clock is used (active for instance) to a mode where it is not used (deep sleep for instance).

Trimming

The WLAN system supports a default inaccuracy of its system clock (hence the radio LO) of up to ±20 ppm. The ACC1340 device is able to handle a higher inaccuracy of its reference clock up to ±50 ppm. A correction is then applied in the block that derives the system clock from the reference clock. In this case, the correction value needs to be provided to the ACC1340. This trimming is supported in the three cases; when this clock is provided to the device either as a digital square wave input, a sinusoidal low amplitude signal, or is generated using a crystal directly connected to the device.

Clock request signals

To minimize power consumption, a clock request output feature is available so that the reference clock can be stopped when not needed by the WLAN system. The clock request output signal can be active high or active low, and the ACC1340 supports internal propagation of a clock request input signal coming from another device in the system. The clock request input shall always be active high. When the reference clock is generated from an external crystal directly connected to the device, these clock request signals are not used.

Different configurations as described below are supported immediately after reset and in all modes of operation, provided that V_{DD_IO} is available.
The clock request functionality is based on three signals: CLKREQOUT1 and CLKREQIN1, with the following function.

- CLKREQOUT1: active high clock request output. Support for either push-pull or open drain output.
- CLKREQIN1: active high clock request input from another device.

External XTAL and built-in oscillator

Table 19. External crystal characteristics requirements

Parameter	Conditions	Min	Typ	Max	Unit
External crystal nominal frequency list			38.4, 40, 52		MHz
Crystal mode			Series		
Crystal drive level		-	-	100	µW
Crystal ESR		-	-	50	Ω
Crystal frequency accuracy at nominal temperature	Reference: 25 °C	-10	0	+10	ppm
Crystal pullability		10	-	150	ppm/pF
Crystal drift due to ageing	After 5 years	-3	0	+ 3	ppm
Crystal drift due to temperature	Reference: 25 °C Range: -30 °C to +85 °C	-12	0	+12	ppm
Load capacitance		-	8	-	pF

The XTAL oscillator is a DCXO. With the XTAL properties mentioned in *Table 19*, the initial frequency accuracy can be tuned down to 2 ppm. Combined with the ageing and temperature drift, this leads to a 20 ppm maximum offset of the local oscillator. This tuning requires an accurate reference that can be provided during production for instance.

2.5.2. Low power clock (sleep clock)

This clock is used for the low power modes of the WLAN systems. If an external low power clock source is used, it must be available after power-up and before the reset is released. It must also remain active all the time until the chip is powered off. If no such external clock source is detected when the reset is released, an internal oscillator will be started and used as a low power clock source.
This clock is provided to the device through a standard digital input, LP_CLK, with default characteristics. The input contains a Schmitt trigger and does not contain any pull.

Table 20. Low power clock requirements

Symbol	Parameter	Min	Typ	Max	Unit
F_{IN}	Frequency	-	32.768	-	kHz
F/F_{IN}	Frequency accuracy	-1000	-	+1000	ppm
Duty cycle		30	-	70	%
Rin	Input resistance	1	-	-	MΩ
Cin	Input capacitance	-	-	5	pF
Jitter	Cycle-to-cycle	-40	-	+40	ns
V_{IL}	ACC1340 input low voltage on LPCLK	0	-	0.2	V
V_{IH}	ACC1340 input high voltage on LPCLK	V_{DD_IO} - 0.2	-	V_{DD_IO}	V
Tr/Tf	Rise and fall time	-	-	500	ns

2.6. Digital interfaces

2.6.1. General control signals

The ACC1340 supports several control signals that have impact on the operation of the full device (not dedicated to a specific function). Some of these signals are available by default on a pin, others can be mapped to a programmable pin.

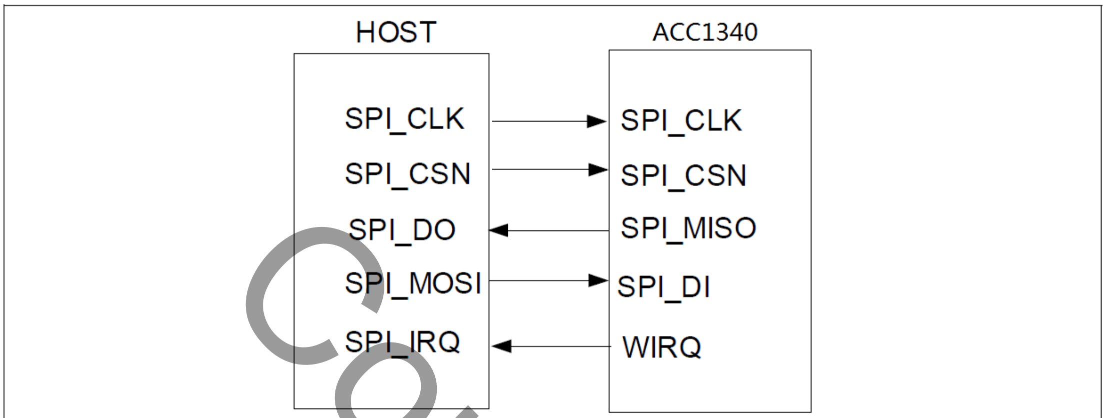
Table 21. Control signals

Signal	Direction	Function
WRESETN	input	RESET of the WLAN subsystem.
CLKREQOUT1	(open drain) output	Signal that requests the reference clock only when needed to allow power saving. See External Clock Source for details on the signal behavior. When the signal is not asserted, the output is converted to a high Z mode. This way, several clock requests can be combined with a passive resistor.
CLKREQIN1	input	Signal that allows the sharing of the reference clock between several devices on a board without the need of external components for the control of the enable of this clock. If this function is not used, the pin may be reused for other functions after reset (PA_SD as part of an LTE coexistence interface for instance). See External Clock Source for details on the signal behavior.
WHOSTSEL	input	Configuration pin used to select the ATE test mode. This pin shall be strapped to GND for normal operation.
HIF5	input/output	The state of this pin is monitored on the rising edge of WRESETN. – LOW selects SPI – HIGH selects SDIO Setup and hold time are those of the SDIO interface

2.6.2. SPI interface

The physical SPI interface is a five-wire data interface: SPI_CSN, SPI_CLK, SPI_DO, SPI_DI, and SPI_INT.

Figure 8. SPI interface



The five signals of the SPI interface are the following:

- SPI_CSN: device select allows the use of multiple slaves (one device select per slave).

This signal is active low. This signal is mandatory, even with only one slave because the host must drive this signal to indicate SPI frames.

- SPI_CLK: clock signal, active for a multiple of data length cycles during an SPI transfer (SPI_CSN active). The clock is allowed to be active when SPI_CSN is not active to serve other slaves.
- SPI_DO: data transfer from slave to master. Data is generated on the negative edge of SPI_CLK by the slave and sampled on the positive edge of SPI_CLK. When SPI_CSN is inactive, this ACC1340 output is in tristate mode.
- SPI_DI: data transfer from master to slave. Data is generated on the negative edge of
- SPI_CLK by the master and sampled on the positive edge of SPI_CLK.
- SPI_IRQ: interrupt from the slave used to request an SPI transfer by the slave to the master. The signal is active high (host input must be level sensitive).

The SPI interface has the following characteristics:

- The maximum operating frequency is 52 MHz. The SPI interface in the ACC1340 supports the timings defined below.
- The SPI interface is operating in half duplex mode.
- The SPI interface is master at the host side, and slave at the ACC1340 side.
- The SPI data length, endianness, and flow control are configurable. The host can change the configuration by writing in the SPI configuration register.

- 16-bit and 32-bit word lengths are supported including the following configurable modes where [bn] is the bit transmission order from left to right:
  - 32-bit Mode0: [b15-b8], [b7-b0], [b31-b24], [b23-b17]
  - 32-bit Mode1: [b31-b24], [b23-b17], [b15-b8], [b7-b0]
  - 32-bit Mode2: [b7-b0], [b15-b8], [b23-b17], [b31-b24]
  - 16-bit Mode0: [b15-b8], [b7-b0]
  - 16-bit Mode1: [b7-b0], [b15-b8]
- Rising clock edge is used for sampling. Active clock edge for shifting is configurable
- Supports automatic indirect addressing of device internal memory using fixed address
- SPI register to facilitate bulk DMA transfer
- Supports host wake up of the WLAN block by SPI register access

The default WLAN SPI configuration is:

- 32-bit data length
- Most significant byte first, default is little endian
- Most significant bit first
- Flow control on SPI_DO and in a register

Figure 9. Default SPI data transfer from the host (master) to the ACC1340 (slave)

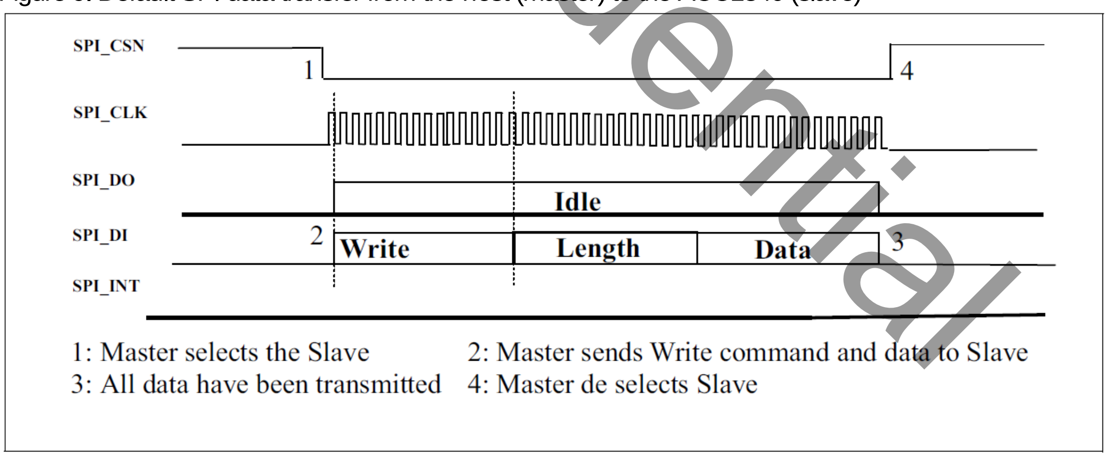


Figure 10. Default SPI data transfer from the ACC1340 (slave)

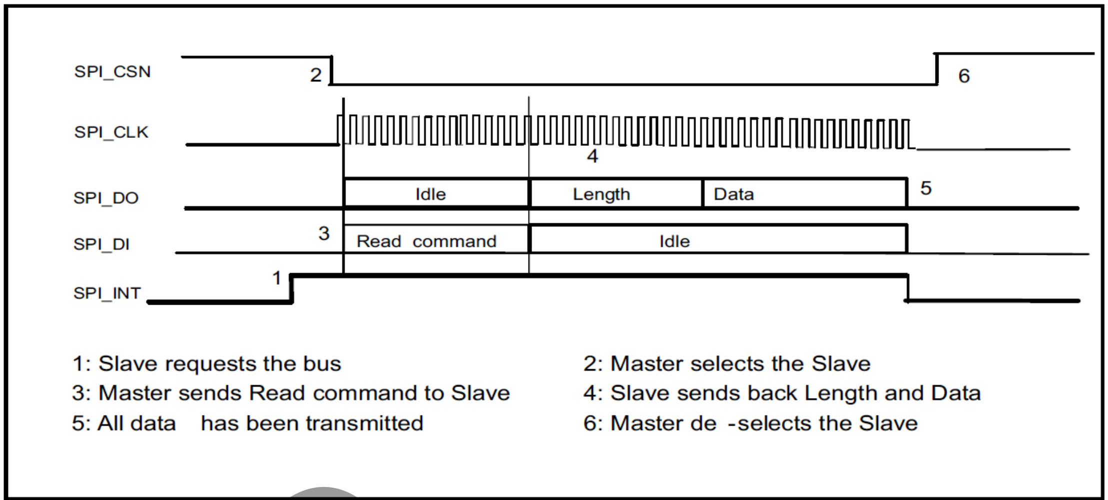


Figure 11. SPI setup and hold timing

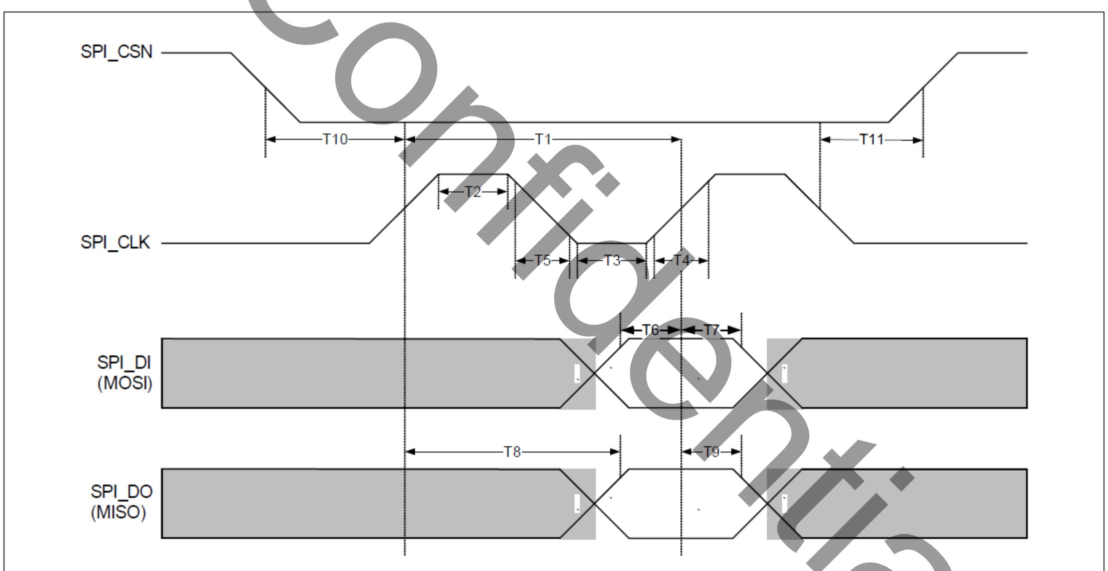


Table 22. SPI timing parameters

Symbol	Description	Min	Typ	Max	Unit
T1	Clock period	19.23[(1)]	-	-	ns
T2 and T3	Clock high and low duration	(0.45 * T1) - T4	-	(0.55 * T1) - T4	ns
T4 and T5	Clock rise and fall time (10% to 90%)	1	-	2.5	ns
T6	Input setup time (SPI_DI valid to SPI_CLK active edge)	5.0	-	-	ns
T7	Input hold time (SPI_CLK active edge to SPI_DI invalid)	3.0	-	-	ns
T8	Output setup time (SPI_CLK active edge SPI_DO valid)	-	-	14.23[(2)]	ns
T9	Output hold time (SPI_CLK active edge to SPI_DO invalid)	3.0	-	-	ns
T10	CSN to clock (CSN fall to 1st rising edge)	5.0	-	-	ns
T11	Clock to CSN (Last falling edge of SPI_CLK to CSN rising edge)	1.0	-	-	ns

1. 19.23 ns = 1/52 MHz
2. 14.23 ns = 19.23 ns – 5 ns

2.6.3. SDIO interface

The SDIO interface is a four-wire to six-wire data interface (SDIO_CLK, SDIO_CMD, SDIO_DATA0, SDIO_DATA1/INT, optional SDIO_DATA2 and SDIO_DATA3). The SDIO interface is compatible with the SDIO specification version 1.10, with the exception that:

- The voltage range is not SD compatible but is compatible with the standard I/O levels defined in this document.
- Interrupt may be generated to the host in four-bit SDIO mode even with no SDIO clock, maximum clock frequency is 50 MHz.

The six signals of the SDIO interface are the following:

- SDIO_CLK: clock signal.
- SDIO_CMD: bidirectional SDIO command line.
- SDIO_DATA0: bidirectional data line.
- SDIO_DATA1/INT: bidirectional data line. When no data is present on the line, it is used as interrupt from the slave, used to request an SDIO transfer from the slave to the master.
- SDIO_DATA2: optional bidirectional data line.
- SDIO_DATA3: optional bidirectional data line.

In case the host does not support an in-band interrupt signal, an optional seventh signal can be used for that purpose:

- WLAN_IRQ may optionally compliment (duplicate) the interrupt function of SDIO_DATA1.

The SDIO interface has following characteristics:

- The maximum operating frequency is 50 MHz. The SDIO interface in the ACC1340 supports the timing defined below.
- The SDIO interface is master at the host side, and slave at the ACC1340 side.

- Operation in SD mode from one to four data bits.

Figure 12. SDIO interface timing

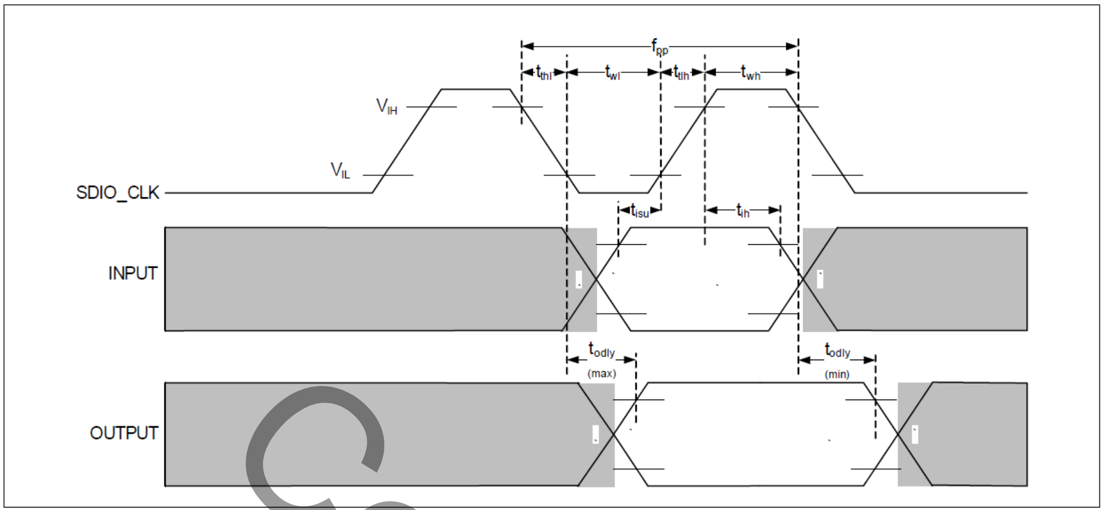


Table 23. SDIO interface timing

Symbol	Parameter	Min	Typ	Max	Unit
f_{pp}	Clock frequency (data transfer mode)	0	-	50	MHz
t_{thl}	Clock fall time	-	-	3	ns
t_{tlh}	Clock rise time	-	-	3	ns
t_{wl}	Clock low time	7	-	-	ns
t_{wh}	Clock high time	7	-	-	ns
t_{isu}	Input setup time	5	-	-	ns
t_{ih}	Input hold time	5	-	-	ns
t_{odly}	Output delay time (during data transfer mode)	-	-	14	ns
t_{OH}	Output hold time	2.5	-	-	ns

2.6.4. FEM control signals

The ACC1340 has five dedicated IOs to control the state of the front-end module and or antenna switch.

Four of the IOs are reserved to control the TX/RX antenna switch for the 2.4 GHz/5 GHz frequency band. The IO that is used to enable the 5 GHz TX switch will also be used to control the 5 GHz PA enable signal. The matching of the four IOs to the four functions is programmable software. Typically the four IOs will be allocated in a way that makes the board layout easier. The behavior of those IOs is controlled by PTA during normal operation. All IOs are configured as input and kept low by a pull-down resistor when the ACC1340 is reset.

The fifth IO is reserved for the control of the BT switch. The behavior of this IO is controlled by the PTA block even when the ACC1340 is reset. This guarantees that BT can access the media on request when WLAN is reset.

Table 24. Control signals

Signal	Direction	Function (control of antenna switch)
FEM_CTRL_1 FEM_CTRL_2 FEM_CTRL_3 FEM_CTRL_4	output	2.4 GHz TX or 2.4 GHz RX or 5 GHz TX (and 5 GHz PAEN) or 5 GHz RX Software programmable
FEM_CTRL_5	output	BT

2.6.5. PTA interface

Bluetooth and WLAN occupy the same 2.4 GHz ISM band that may lead to interference when operating concurrently. The IEEE standard 802.15.2 recommends a collaborative coexistence mechanism of Packet Traffic Arbitration (PTA) based on time-sharing BT and/or WLAN requesting the medium before any communication. In case of conflict, PTA decides whom to award the medium to, based on priority of the BT and WLAN traffic and their current status. By using the coexistence mechanism, it is possible to dynamically allocate bandwidth to the two devices when simultaneous operations is required while the full bandwidth can be allocated to one of them in case the other does not require activity.

The combination of time division multiplexing and the priority mechanism avoids the interference due to packet collision. It also allows the maximization of the 2.4 GHz ISM bandwidth usage for both devices while preserving the quality of some critical types of link. A typical application would be to guarantee optimal quality to the Bluetooth voice communication while an intensive WLAN communication is ongoing.

The ACC1340 implements the IEEE 802.15.2 recommended practices referred to as standard PTA. The ACC1340 also implements further enhancements based on proprietary hardware and algorithms, known as ePTA. The ACC1340 also implements other simpler alternatives for compatibility with less advanced counter-parts.

2.7. RF inputs and outputs

2.7.1. Electrical characteristics

Table 25. Electrical characteristics of RF inputs and outputs

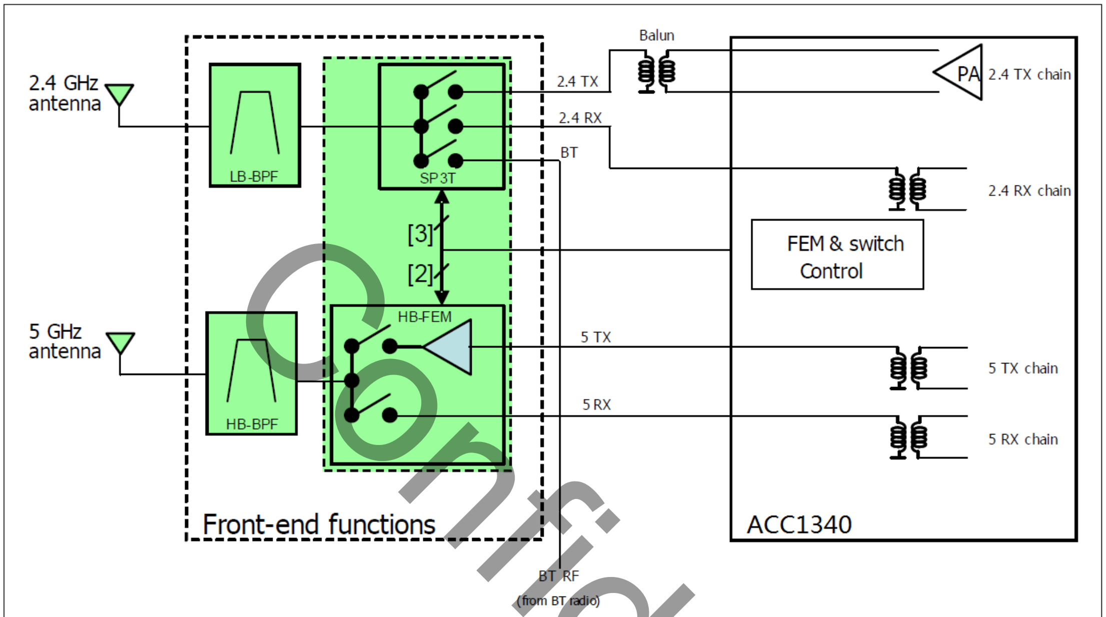
Ball name	Type	$Z_{characteristic}$ typ, ohm(1)	Dedicated frequency range MHz
RF_IN_LB	Single-ended	50	2.4 - 2.4835
RF_IN_HB	Single-ended	50	4.9 - 5.825
RF_OUT_LB_1	Differential	20 + 9j	2.4 - 2.4835
RF_OUT_LB_2	Differential		2.4 - 2.4835
RF_OUT_HB	Single-ended	50	4.9 - 5.825

1. This part of the circuit is biased. Unused portions of the circuit are powered down. The impedance might differ.

2.7.2. Reference schematic

Figure 15 gives a simplified view of the components to be placed between RF ports and the antenna.

Figure 15. Schematic of the antenna interface for a dual-band operation



3. WLAN functional description

The WLAN subsystem implements the MAC and physical layer functionalities of the 802.11 specification and amendments. The radio is capable of operation in all of the available channels in the 2.4 GHz and 5 GHz frequency bands.

The WLAN radio is based on a direct conversion architecture with two RF front-ends for operation in 2.4 GHz (low) and 5 GHz (high) bands and a common analog and digital baseband. The radio is designed to be operational either in the high band or the low band.

The digital transceiver implements the OFDM (802.11a/g/n) and DSSS/CCK (802.11b/g) functions, supporting the following PHY features

- OFDM
  - Bandwidth: 20 MHz
  - Modulations: BPSK, QPSK, 16QAM, and 64QAM
  - Code rates: 1/2, 3/4, and 5/6
  - Preambles: legacy, greenfield, and mixed mode preambles
  - Single convolutional encoder
  - Reception of 802.11n 2x1 STBC encoded signals for range enhancement
  - Reception of 802.11n beam formed and channel sounding packets (support for maximum of two transmitter preambles)
  - RIFS of 2 μs (802.11n only)
- DSSS/CCK
  - Modulations: DBPSK, DQPSK, and CCK
  - Preambles: long and short

3.1. Modem receiver

The low and high band signals are demodulated by separate RF front-ends. The radio signal from the balanced 2.4 GHz or 5 GHz RF input is amplified by the low band or high band LNA. The passive receive switching mixers are driven by quadrature LO signals supplied by the on-device RF PLL. The amplified mixer output is fed to a common analog baseband circuit. The analog baseband receiver performs part of the channel filtering and further signal amplification, such that the signal is presented at the correct range of the A/D converter. High-speed sigma delta A/D converters are employed for signal sampling. High over-sampling ratio and noise shaping techniques provide high dynamic range, thereby reducing the analog complexity. The rest of the channel filtering and gain amplification is performed in the digital domain. DC compensation is performed partly in the analog and partly in the digital domain. AGC control, DC tracking and control, quadrature imbalance tracking, and control are implemented digitally. The RC time constants for the analog filters are calibrated automatically.

OFDM and DSSS/CCK signals are coherently demodulated and decoded by the digital modem. The digital modem also implements the CCA 802.11h/k functions to collect the link statistics such as, RSSI, RPI, IPI, and RSNI.

3.2. Modem transmitter

The digital modem implements the OFDM and DSSS/CCK modulation for all frame-formats specified for a single layer/transmitter. The OFDM and DSSS/CCK modulated I/Q signals use a common circuit for digital up-sampling, filtering, quadrature imbalance compensation, LO leakage correction, and digital power scaling. High speed sigma delta D/A converters are employed for digital to analog conversion reducing the analog complexity. The filtered analog I/Q signals are up-converted using separate low and high band modulators. The modulator is driven by the signal from the LO buffer/dividers supplied by VCO. The up- converted RF signals are further amplified by a digitally controlled amplifier. The low band TX path integrates a power amplifier, eliminating the need for any external amplification between the transceiver and the antenna.

Transmit I/Q calibration is implemented partly in both the analog and digital domains. The transmitter implements automatic level control taking into account the desired output power and PA's working conditions (temperature, supply, modulation).

3.3. RF PLL

A single RF LC oscillator PLL provides the quadrature LO signals to the low and high band up and down converters. A fractional synthesizer design is employed to accommodate different reference frequencies. The loop filter is fully integrated inside the ACC1340.

3.4. WLAN controller

The main components of the WLAN controller are the CPU subsystem, the MAC protocol accelerator subsystem, encryption/decryption engines, host interfaces, and an enhanced PTA for WLAN/BT coexistence.

3.5. IEEE 802.11 standard compliance and support

3.5.1. General support

Support for operation in 802.11b, 802.11a, 802.11g, and 802.11g networks, meaning support for basic mandatory MAC features and for the mandatory modes of:

- Clause 15, DSSS PHY (basic 802.11)
- Clause 17, OFDM PHY (802.11a)
- Clause 18, HR/DSSS PHY (802.11b)
- Clause 19, ERP PHY (802.11g)
- Clause 21, HT PHY (802.11n), compliant to Wi-Fi handset profile

Support for operation as a wireless station (STA) in both infrastructure and ad-hoc networks; in particular, the module supports IBSS operation and also implements support for IBSS power save mode.

3.5.2. International regulatory support

Supports the IEEE 802.11d standard amendment for regulatory domain identification. Supports the IEEE 802.11h standard amendment for Dynamic Frequency Selection (DFS), Transmit Power Control (TPC), and spectrum management.

3.5.3. Radio resource management support

Supports the mandatory aspects introduced in the IEEE 802.11k amendment to the standard.

3.5.4. Security support

Support for basic WEP:

- Supports key lengths of 40, 104 bits for WEP encryption (IV generation and ICV verification)
- Open and shared key authentication.
- Cryptographically weak IVs are avoided

Supports the MAC mandatory aspects of RSNA security including TKIP and AES-CCMP and the following optional security features:

- RSNA for IBSS is supported

Supports protected management frames introduced in IEEE 802.11w amendment to the standard.

- CCMP for unicast management frames
- BIP for broadcast/multicast management frames

Supports fast BSS transition in a RSNA introduced in the IEEE 802.11r amendment to the standard.

3.5.5. Quality of service

Supports the EDCA medium access method, four access categories, and TSPEC signaling.

3.5.6. Power saving

Support for basic PSM.

Support for Unscheduled-Automatic Power Save Delivery (U-APSD) as defined by WMM- PS.

3.5.7. Fast roaming

Supports fast BSS transition introduced in the IEEE 802.11r amendment to the standard.

3.5.8. 802.11n

Supports MAC enhancements for higher throughput as defined in the IEEE 802.11n amendment to the standard.

3.5.9. Wi-Fi alliance interoperability testing

General support

The device when built into a system has sufficient features and performance to be passed by Wi-Fi as an ASD (Application Specific Device).

International regulatory support

Support for DFS and TPC (802.11h).

Security support

Support for WEP, WPA, WPA2. The device also includes support for PMF.

Quality of service

Support for WMM (EDCA from 802.11e), WMM-PS (U-APSD from 802.11e, with interface for Tspec negotiation by upper layers).

High throughput

The device supports the mandatory features defined in the TGn MRD for the HH (Handheld) market segment.

Wi-Fi protected setup

For easy configuration

Wi-Fi Direct support

The device supports both Group Owner (GO) and Group Client (GC) modes. Additionally the device also supports concurrent Wi-Fi and Wi-Fi Direct operation.

3.6. Regional regulatory standards compliance

Following is a non-exhaustive list of regional regulatory standards which the ACC1340 complies with. For some of the standards, it is assumed that the ACC1340 is used together with the approved components part of the reference design (see ACC1340 Hardware user manual).

Table 26. Regional regulatory approvals

Region	Regulatory authority	Specification	Reference in FCC, ETSI / EN and TELEC standards
US and Canada	FCC / IC	FCC Part 15, Subpart C	Section 15.205: Restricted bands of operation
			Section 15.209: Radiated emission limits, general requirements (EIRP)
			Section 15.247: Operation within the bands 902 - 928 MHz, 2400 - 2483.5 MHz, and 5725 – 5850 MHz
EU	ETSI / EN	EN300 328: 2.4 GHz ISM band operation	Section 4.3.1 to 4.3.4: maximum transmit power, maximum EIRP spectral density, frequency range and frequency hopping
			Section 4.3.6 to 4.3.7: Transmit and receive spurious emissions
		EN 301 893: 5 GHz band operation	Section 4.2 to 4.6: Center frequency, occupied channel bandwidth, transmit power and transmit power density, TX and RX unwanted or spurious emissions
Japan	TELEC (former MKK)	ARIB STD T66 (b/g)	Section 3.1, 3.2, 3.3, technical requirements on radio equipment, general, TX and RX.
		RCR STD T33 (b)	-
		ARIB STD T71 (a)	-
		ARIB STD T70 (a/j)	-

3.7. Low power modes

Table 27. WLAN low power modes

Low power mode	Description
Standby (Complete power down)	W_RESETN is active and WLAN subsystem is effectively powered down
Sleep	The WLAN subsystem: – Is largely powered down – Operates from the low power clock (sleep clock) (32 kHz) – Preserves the value of internal state variables and the CPU firmware – Does not accept commands from the host – Limited access to clock stabilization time, interrupt source to the host, WLAN wakeup registers – Reference clock is not active in any part of the design
PSM	The WLAN subsystem: – Is partly powered down depending on the WLAN activity – Accepts commands from the host – Reference clock is active depending on the active mode – Dynamically switches between sleep and active mode when needed
Active	The WLAN subsystem – The CPU subsystem and the host interface are active – The system is transmitting or receiving
Rx-Idle	The WLAN subsystem – Is listening to the channel. All TX circuits are disabled (clocks are switched off). Only minimum necessary RX circuits are enabled.

3.8. Host interface

The WLAN host interface may be either SPI or SDIO.

3.9. PTA

Bluetooth, WLAN 802.11b and 802.11g technologies occupy the same 2.4 GHz ISM band. The ACC1340 implements a set of mechanisms to avoid interference in a collocated scenario.

When configured according to “enhanced PTA”, the ACC1340 implements proprietary features that further optimize coexistence. Advanced information on the Bluetooth traffic is communicated via a serial protocol on the four wires defined for standard PTA.

3.10. WLAN – LTE coexistence

WLAN and LTE use adjacent frequency bands. The ACC1340 implements mechanisms to minimize the interference between the two systems using a three-signal interface:

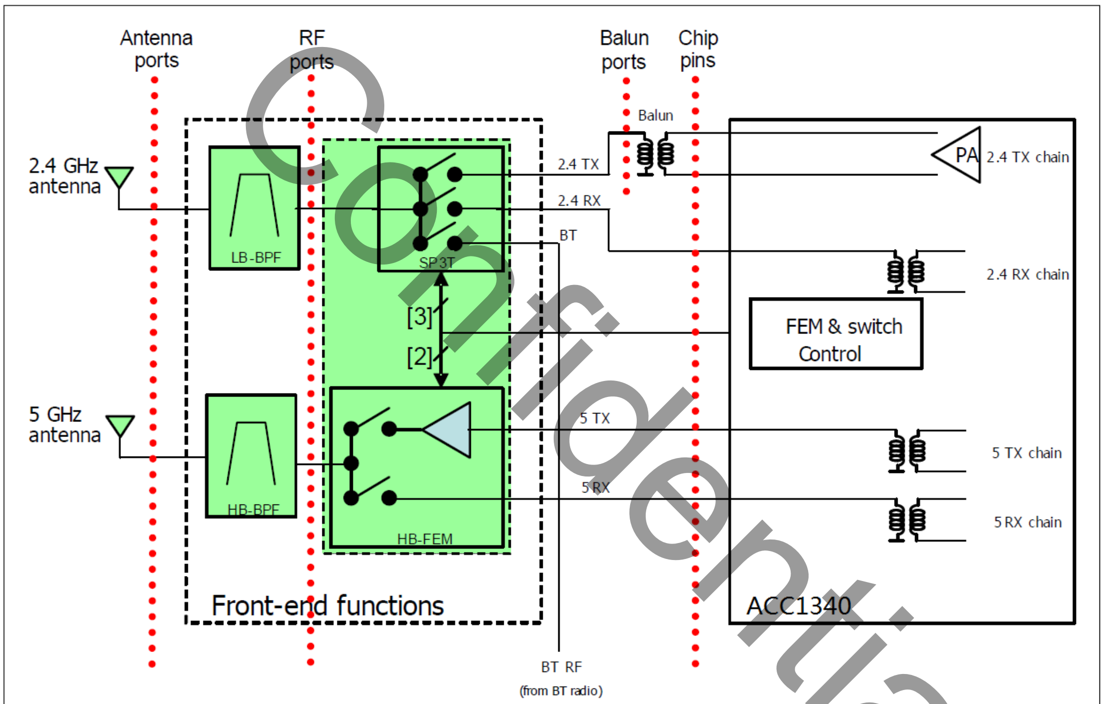
- WLAN_ACTIVITY that signals upcoming high importance WLAN activity
- LTE_INACTIVITY that signals LTE upcoming absence of activity to guarantee a minimum WLAN throughput
- PA_SD that signals upcoming LTE reception (hence the need to stop WLAN transmission activity)

4. WLAN transceiver performances

4.1. RF receiver performance

This section specifies the performances of the RF receiver referred to the input pins of the ACC1340 (called chip pins) and gives indications of the performances at the antenna port or the RF port depending on which is the most relevant. For the 2.4GHz band, this indication is obtained considering an attenuation of 3.5 dB between the antenna port and the chip pins. And for the 5GHz band, 2.5 dB between the antenna port and chip pins. This corresponds to what is measured on the ACC1340 reference design including the switch, band-pass filter, and track losses, but without the 5GHz FEM's LNA.

Figure 16. Definition of the chip pins, RF port and antenna port



4.1.1. Maximum input signal level

Table 28. Maximum input signal levels at the RF port

Mode	Para-meter	Conditions / comments	Specification at the RF port			
			Min	Typ	Max	Unit
2.4 GHz (802.11g/n)	Maximum input	Max bit rate @ PER < 8% for CCK/DSSS	-	-	-19.5	dBm
2.4 GHz (802.11g/n)	Maximum input	Max bit rate @ PER < 10% for OFDM	-	-	-19.5	dBm
5 GHz (802.11a/n)	Maximum input	Max bit rate @ PER < 10%	-	-	-30.5	dBm

4.1.2. Minimum input signal level (sensitivity)

Table 29. 2.4 GHz sensitivity (minimum input level) at the RF port

Band	Standard	Rate [Mbps]	Modulation	Coding	Conditions	Specification at the RF port			Units
						Min	Typ(1)	Max(2)(3)	
2.4 GHz	DSSS/CCK	1	DSSS	-	@ PER<8% 1024 bytes per frame, full operating range	-	-98.00	-96.00	dBm
		2	DSSS	-		-	-95.00	-93.00	dBm
		5.5	CCK	-		-	-93.00	-91.00	dBm
		11	CCK	-		-	-91.50	-90.00	dBm
	11g/n (20 MHz, OFDM)	6	BPSK	1/2	@ PER<10% 1000 bytes per frame, full operating range	-	-93.50	-92.00	dBm
		9	BPSK	3/4		-	-91.50	-90.00	dBm
		12	QPSK	1/2		-	-90.50	-89.00	dBm
		18	QPSK	3/4		-	-88.00	-87.00	dBm
		24	16QAM	1/2		-	-85.50	-84.00	dBm
		36	16QAM	3/4		-	-82.00	-81.00	dBm
		48	64QAM	2/3		-	-78.00	-76.00	dBm
		54	64QAM	3/4		-	-76.50	-75.00	dBm
	11n (OFDM, 20 MHz, Nss = 1)	6.5	BPSK	1/2	@ PER<10% 4096 bytes per frame, full operating range	-	-92.00	-91.00	dBm
		13	QPSK	1/2		-	-89.00	-88.00	dBm
		19.5	QPSK	3/4		-	-86.50	-85.00	dBm
		26	16QAM	1/2		-	-84.00	-83.00	dBm
		39	16QAM	3/4		-	-80.50	-79.00	dBm
		52	64QAM	2/3		-	-76.50	-75.00	dBm
		58.5	64QAM	3/4		-	-74.50	-73.00	dBm
		65	64QAM	5/6		-	-73.00	-72.00	dBm

1. There is a derating of 1.5 dB on channel 1 and 0.75 dB on channel 2.
2. Sensitivity decreases with higher temperature with 0.01 dB/C.
3. Maximum limits apply from -30 °C to +55 °C. At +85 °C, maximum derates with 0.03 dB

Table 30. 5 GHz sensitivity (minimum input level) at the RF port

Band	Standard	Rate [Mbps]	Modulation	Coding	Conditions	Specification at the RF port			Units
						Min	Typ	Max	
5 GHz	11a/n (OFDM, 20 MHz)	6	BPSK	1/2	@ PER<10% 1024 bytes per frame, full operating range	-	-93	-89.5	dBm
		9	BPSK	3/4		-	-91	-87.5	dBm
		12	QPSK	1/2		-	-90	-86.5	dBm
		18	QPSK	3/4		-	-87.5	-84	dBm
		24	16QAM	1/2		-	-84.5	-81.5	dBm
		36	16QAM	3/4		-	-81.5	-78	dBm
		48	64QAM	2/3		-	-77.5	-73.5	dBm
		54	64QAM	3/4		-	-75.5	-72	dBm
	11n (OFDM, 20 MHz, Nss = 1)	6.5	BPSK	1/2	@ PER<10% 4096 bytes per frame, full operating range	-	-91	-88	dBm
		13	QPSK	1/2		-	-88	-85	dBm
		19.5	QPSK	3/4		-	-85.5	-82	dBm
		26	16QAM	1/2		-	-83	-79.5	dBm
		39	16QAM	3/4		-	-79.5	-76.5	dBm
		52	64QAM	2/3		-	-75.5	-72	dBm
		58.5	64QAM	3/4		-	-74	-70	dBm
		65	64QAM	5/6		-	-72.5	-68	dBm

4.1.3. Adjacent channel rejection and blockers

Table 31. 802.11a/g adjacent channel rejection at antenna port

Mode	Modulation and coding scheme	Minimum sensitivity level [dBm]	Conditions/ comments	Indication at antenna port			
				Min	Typ	Max	Unit
OFDM (802.11a/g)	BPSK 1/2	-82	Tests as specified in IEEE 802.11, Clause 17.3.10.2	**16**	**21**	**-**	**dBc**
	BPSK 3/4	-81		**15**	**20**	**-**	**dBc**
	QPSK 1/2	-79		**13**	**18**	**-**	**dBc**
	QPSK 3/4	-77		**11**	**16**	**-**	**dBc**
	16QAM 1/2	-74		**8**	**13**	**-**	**dBc**
	16QAM 3/4	-70		**4**	**9**	**-**	**dBc**
	64QAM 2/3	-66		**0**	**5**	**-**	**dBc**
	64QAM 3/4	-65		**-1**	**4**	**-**	**dBc**

Table 32. 802.11n adjacent channel rejection at antenna port

Mode	Modulation and coding scheme	Minimum sensitivity level [dBm]	Conditions/ comments	Indication at antenna port			
				Min	Typ	Max	Unit
OFDM (802.11n)	BPSK 1/2	-82	Tests as specified in IEEE P802.11n-2009	**16**	**21**	**-**	**dBc**
	QPSK 1/2	-79		**13**	**18**	**-**	**dBc**
	QPSK 3/4	-77		**11**	**16**	**-**	**dBc**
	16QAM 1/2	-74		**8**	**13**	**-**	**dBc**
	16QAM 3/4	-70		**4**	**9**	**-**	**dBc**
	64QAM 2/3	-66		**0**	**5**	**-**	**dBc**
	64QAM 3/4	-65		**-1**	**4**	**-**	**dBc**
	64QAM 5/6	-64		**-2**	**3**	**-**	**dBc**

Table 33. DSSS/CCK (802.11b/g) adjacent channel rejection

Mode	Data rate	Minimum sensitivity level [dBm]	Conditions/comments	Indication at antenna port[1]			
				Min	Typ	Max	Unit
DSSS/CCK	11 Mbps	-76	At 25 MHz offset, 11 Mbps	**35**	**38**	**-**	**dBc**

4.1.4. Non-adjacent channel rejection

Table 34. 802.11a/g non-adjacent channel rejection

Mode	Modulation and coding scheme	Minimum sensitivity level [dBm]	Conditions/ comments	Indication at antenna port			
				Min	Typ	Max	Unit
OFDM (802.11a/g)	BPSK 1/2	-82	Tests as specified in IEEE 802.11, Clause 17.3.10.3	**32**	**39**	**-**	**dBc**
	BPSK 3/4	-81		**31**	**38**	**-**	**dBc**
	QPSK 1/2	-79		**29**	**36**	**-**	**dBc**
	QPSK 3/4	-77		**27**	**34**	**-**	**dBc**
	16QAM 1/2	-74		**24**	**31**	**-**	**dBc**
	16QAM 3/4	-70		**20**	**27**	**-**	**dBc**
	64QAM 2/3	-66		**16**	**23**	**-**	**dBc**
	64QAM 3/4	-65		**15**	**22**	**-**	**dBc**

Table 35. 802.11n non-adjacent channel rejection

Mode	Modulation and coding scheme	Minimum sensitivity level [dBm]	Conditions/ comments	Indication at antenna port			
				Min	Typ	Max	Unit
OFDM (802.11n)	BPSK 1/2	-82	Tests as specified in IEEE P802.11n-2009	**32**	**39**	**-**	**dBc**
	QPSK 1/2	-79		**29**	**36**	**-**	**dBc**
	QPSK 3/4	-77		**27**	**34**	**-**	**dBc**
	16QAM 1/2	-74		**24**	**31**	**-**	**dBc**
	16QAM 3/4	-70		**20**	**27**	**-**	**dBc**
	64QAM 2/3	-66		**16**	**23**	**-**	**dBc**
	64QAM 3/4	-65		**15**	**22**	**-**	**dBc**
	64QAM 5/6	-64		**14**	**21**	**-**	**dBc**

4.1.5. RSSI and RCPI

Table 36. RSSI and RCPI accuracy at the RF port

Parameter	Conditions	Typ	Max	Unit
RSSI accuracy at the RF port	V_{BAT} ≥ 3.6 V, 25 °C, excluding insertion loss variations between the ANT and ACC1340 pins	±2	±3.5	dB
RCPI accuracy at the RF port		±2	±3.5	dB

4.2. RF transmitter performance

This section specifies the performances of the RF transmitter referred to the output of the balun connected to the pins of the ACC1340 and gives indications of the performances at the antenna port or the RF port depending on which is the most relevant. For the 2.4 GHz band, this indication is obtained considering an attenuation of 3.5 dB between output of balun and the antenna port, and 0.7 dB between output of balun and the RF port. For the 5 GHz band, the actual gain of the external PA and the losses of the switch are taken into account between chip pins and the RF port and an attenuation of 1 dB between the RF port and the antenna port.

Output power

The output power is specified as average conducted power at the antenna connector. The output power specifications are met over frequency, temperature, and a battery voltage of 3.6 V upwards according to the full specification operating. In the full specification with output power backed-off (2.7 V < V_{BAT} < 3.6 V) and functional with reduced performance (2.3 V < V_{BAT} < 2.7 V) operating ranges, the output power needs to be backed-off to sustain the transmit EVM, spectral mask, harmonic level, and spurious emissions specifications.

Table 37. Output power vs. EVM for 2.4 GHz at the RF port for 802.11b/g

(VSMPS = 1.8 V)

Modulation	Coding rate	Conditions	Specification at the RF port				EVM		EVM	
			Min	Typ	Max	Unit	Max	Unit	Max	Unit
DSSS/CCK	-	All conditions typical: $V_{BAT} \geq 3.6$ V, VSMPS = 1.8 V, 25 °C, 50 Ω load; meeting spectral mask, EVM, harmonic levels, spurious emissions, and regulatory requirements in general	20.5	21.25	-	dBm	-14.5	dB	18.84	%
BPSK	1/2		20.5	21.25	-	dBm	-14.5	dB	18.84	%
BPSK	3/4		20.5	21.25	-	dBm	-14.5	dB	18.84	%
QPSK	1/2		20.5	21.25	-	dBm	-14.5	dB	18.84	%
QPSK	3/4		20.5	21.25	-	dBm	-14.5	dB	18.84	%
16QAM	1/2		20.5	21.25	-	dBm	-17.5	dB	13.34	%
16QAM	3/4		19.5	20.25	-	dBm	-20.5	dB	9.94	%
64QAM	2/3		18.5	19.25	-	dBm	-23.5	dB	6.68	%
64QAM	3/4		17.5	18.25	-	dBm	-25.5	dB	5.31	%

Table 38. Output power vs. EVM for 2.4 GHz at the RF port for 802.11n

(VSMPS = 1.8 V)

MCS	Conditions or comments	Specification at the RF port				EVM		EVM	
		Min	Typ	Max	Unit	Max	Unit	Max	Unit
MCS-0	All conditions typical: $V_{BAT} \geq 3.6$ V, VSMPS = 1.8 V, 25 °C, 50 Ω load; meeting spectral mask, EVM, harmonic levels, spurious emissions, and regulatory requirements in general	20.5	21.25	-	dBm	-14.5	dB	18.84	%
MCS-1		20.5	21.25	-	dBm	-14.5	dB	18.84	%
MCS-2		20.5	21.25	-	dBm	-14.5	dB	18.84	%
MCS-3		20.5	21.25	-	dBm	-17.5	dB	13.34	%
MCS-4		19.5	20.25	-	dBm	-20.5	dB	9.94	%
MCS-5		18.5	19.25	-	dBm	-23.5	dB	6.68	%
MCS-6		17.5	18.25	-	dBm	-25.5	dB	5.31	%
MCS-7		16.25	17.00	-	dBm	-28.5	dB	3.76	%

Power back-off

- To guarantee meeting spectral mask, EVM, harmonic levels, spurious emissions, and regulatory requirements in general the output power shall be backed-off by:
  - 2.45 dB/V when 3.4 V < V_{BAT} < 3.6 V
  - 3.25 dB/V when 2.7 V < V_{BAT} < 3.4 V
  - 4.25 dB/V when V_{BAT} < 2.7 V
- When the load of the balun is not 50 Ω, the output power is backed off to guarantee meeting spectral mask, EVM, harmonic levels, spurious emissions, and regulatory requirements in general. The amount of back-off needed is given detailed as a function of VSWR.

Table 39. Power back-off as a function of the VSWR at the RF port

Power back-off		VSWR			
Modulation	Coding rate	1.3:1	1.5:1	2:1	3:1
DSSS/CCK	-	-	-	2 dB	3 dB
BPSK	1/2	0.3 dB	0.5 dB	1 dB	2 dB
64QAM	3/4	0.4 dB	0.7 dB	1.5 dB	4 dB

- The device is able to withstand a VSWR of up to 12:1 without any damage.
- When the temperature increases from +25 °C to +85 °C, the output power must be backed off by 0.28 dB per 10 °C increase to guarantee meeting spectral mask, EVM, harmonic levels, spurious emissions, and regulatory requirements in general.

Table 40. Output power vs. EVM for 5 GHz at the RF port for 802.11a

Modulation	Coding rate	Conditions	Specification at the RF port				EVM		EVM	
			Min	Typ	Max	Unit	Max	Unit	Max	Unit
BPSK	1/2	All conditions typical: $V_{BAT} \geq 3.6$ V, 25°C, 50 Ω load; meeting spectral mask, EVM, harmonic levels, spurious emissions, and regulatory requirements in general	19.00	19.50	-	dBm	-14.0	dB	20.03	%
BPSK	3/4		19.00	19.50	-	dBm	-14.0	dB	20.03	%
QPSK	1/2		19.00	19.50	-	dBm	-14.0	dB	20.03	%
QPSK	3/4		19.00	19.50	-	dBm	-14.0	dB	20.03	%
16QAM	1/2		18.00	18.50	-	dBm	-17.0	dB	14.21	%
16QAM	3/4		17.0	17.50	-	dBm	-20.0	dB	10.00	%
64QAM	2/3		16.0	16.50	-	dBm	-23.0	dB	7.0	%
64QAM	3/4		15.00	15.50	-	dBm	-25.0	dB	5.60	%

Table 41. Output power vs. EVM for 5 GHz at the RF port for 802.11n

MCS	Conditions	Specifications at the RF port				EVM		EVM	
		Min	Typ	Max	Unit	Max	Unit	Max	Unit
MCS-0	All conditions typical: $V_{BAT} \geq 3.6$ V, 25°C, 50 Ω load; meeting spectral mask, EVM, harmonic levels, spurious emissions, and regulatory requirements in general	19.00	19.50	-	dBm	-14.0	dB	20.03	%
MCS-1		19.00	19.50	-	dBm	-14.0	dB	20.03	%
MCS-2		19.00	19.50	-	dBm	-14.0	dB	20.03	%
MCS-3		18.00	18.50	-	dBm	-17.0	dB	14.21	%
MCS-4		17.00	17.50	-	dBm	-20.0	dB	10.00	%
MCS-5		16.00	16.50	-	dBm	-23.0	dB	7.06	%
MCS-6		15.00	15.50	-	dBm	-25.0	dB	5.60	%
MCS-7		14.00	14.50	-	dBm	-28.0	dB	3.99	%

Spectral mask

Table 42. Transmit spectral mask at the RF port and antenna port

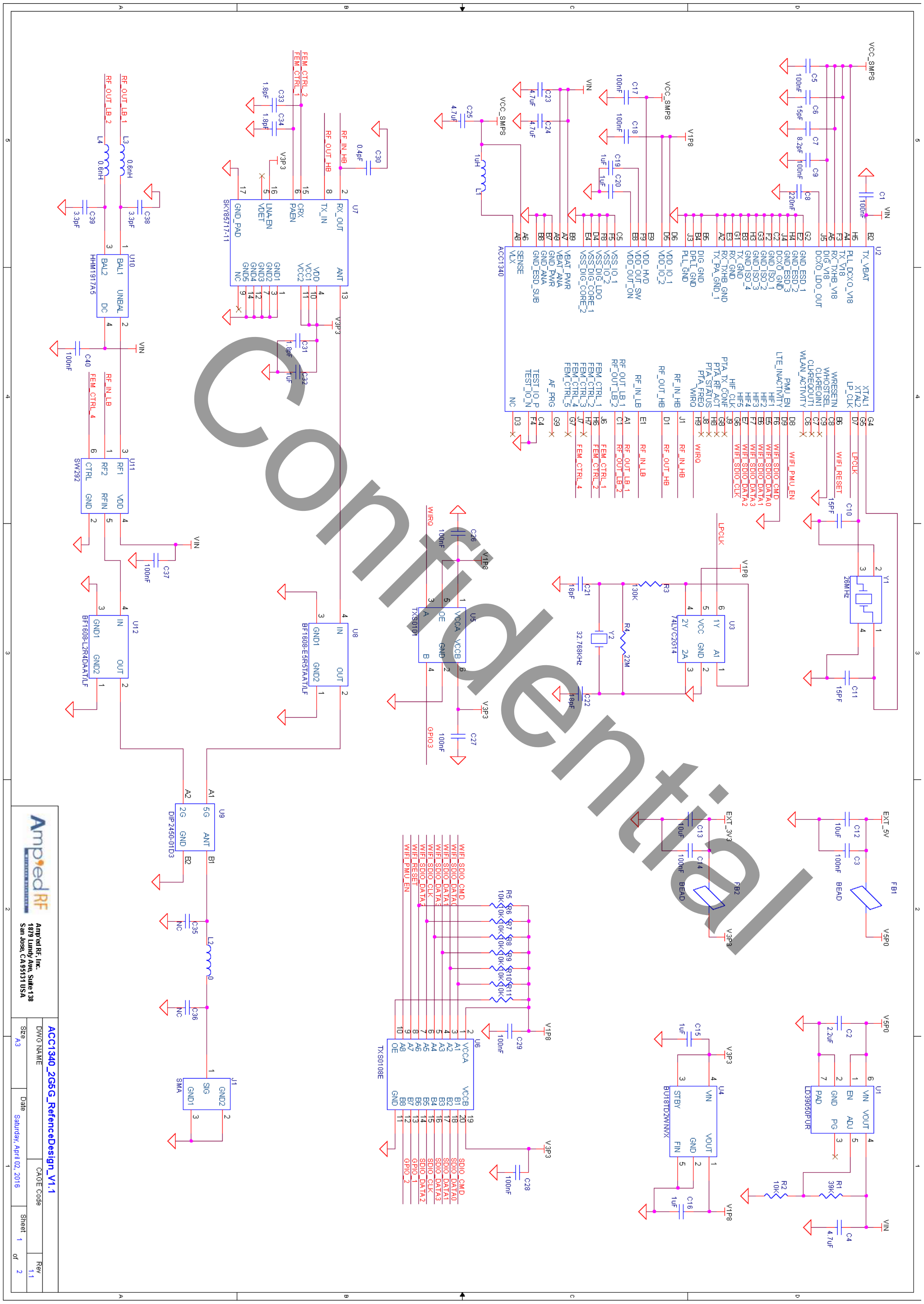
Band	Mode	Parameter	Conditions	Specification			
				Min	Typ	Max	Units
2.4 GHz	DSSS/CCK TX (11b/g)	Spectral mask ±11~22 MHz	Requirements over operating temperature and voltage range	-	-	-30	dBr
		Spectral mask > ±22 MHz		-	-	-50	dBr
	OFDM TX (20 MHz channels, 11g/j/n)	Spectral mask ±11 MHz		-	-	-20	dBr
		Spectral mask ±20 MHz		-	-	-28	dBr
		Spectral mask ±30 MHz		-	-	-45	dBr
5 GHz	OFDM TX (20 MHz channels, 11a/n)	Spectral mask ±11 MHz		-	-	-20	dBr
		Spectral mask ±20 MHz		-	-	-28	dBr
		Spectral mask ±30 MHz		-	-	-45	dBr

Harmonic levels

Table 43. Harmonic levels

Band	Harmonic	Freq [MHz]		Conditions	Emissions		Unit
		Min freq	Max freq		Specification at the RF port	Indication at ANT port(1)	
					Max	Max	
2.4 GHz	2nd	4824	4968	RBW = 1 MHz; Detector = average; Load VSWR <= 3:1 (all phases)	-6	-42.5	dBm/MHz
	3rd	7236	7452		-17.5	-47	dBm/MHz
	4th	9648	9936		-24.5	-44	dBm/MHz
	5th	12060	12420		-29.5	-47	dBm/MHz
5 GHz	2nd	9830	11650		-34.5	-47	dBm/MHz
	3rd	14745	17475		-37.5	-47	dBm/MHz
	4th	19660	23300		-47.5	-47	dBm/MHz

5. Example Application Reference Design



6. Package mechanical data

The device ACC1340 is in lead-free/RoHS-compliant 73-pin WLCSP package.

Figure 17. WLCSP with depopulated pitch and 0.25 mm ball - bottom view

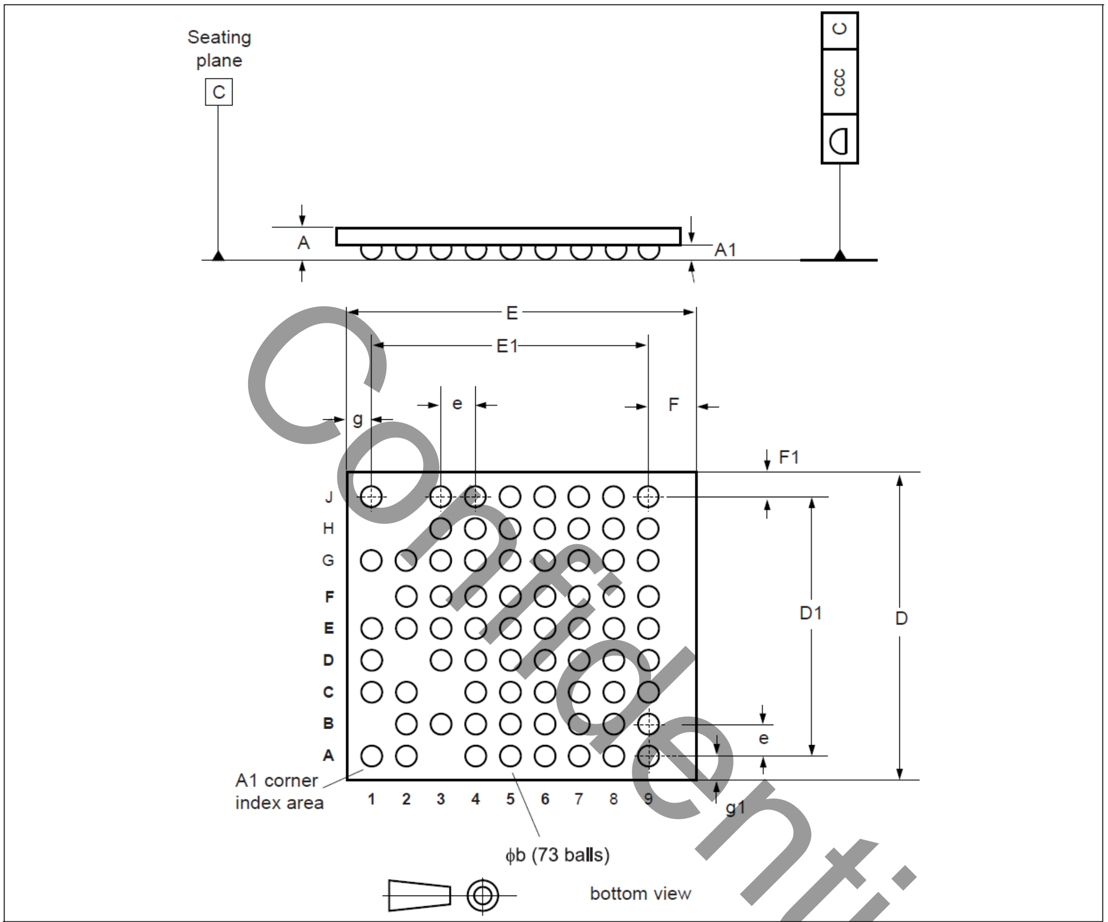


Table 44. Package dimensions

Databook (mm)				
Reference	Min	Typ	Max	Notes
A	0.490	0.545	0.60	Height
A1	0.17	0.20	0.23	-
b	0.24	0.27	0.30	(1)
D	3.80	3.84	3.88	-
D1	-	3.20	-	-
E	4.06	4.10	4.14	-
E1	-	3.20	-	-
e	-	0.40	-	-
F	-	0.60	-	(2)

Databook (mm)				
Reference	Min	Typ	Max	Notes
F1	-	0.32	-	(2)
g	-	0.30	-	(2)
g1	-	0.32	-	(2)

1. The typical ball diameter before mounting is 0.25 mm.
2. The matrix ball array is not centered.

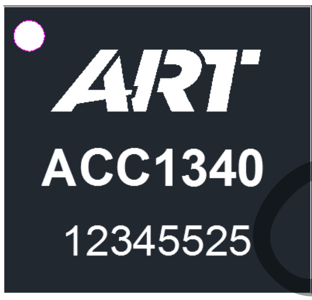


Table 45. Package marking

Item	Description	Format	Value
A	Component identification	-	ACC1340
B	Wafer lot	5 digit	-
C	Package date	3 digit, week/year	-

Table 46. Ordering information

Order code	Description	Package	Packing
ACC1340	802.11abgn dual-band WLAN	CSP	tape and reel

7. Revision history

Date	Revision	Changes
9/29/2015	1.0	First revision
8/11/2016	1.1	Updated reference design
2/6/2018	1.2	Updates to certifications and drawings