ACH1190 Audio Host Processor

Features

- 60-pin lead-free/RoHS compliant
- QFN or BGA package
- ARM Cortex-M4 with floating point processing option
- Two programmable fractional-N synthesizers to reduce interference
  - Supplies CPU clock frequencies, up to max 200MHz
  - Supplies integrated audio codec
- 960k byte internal SRAM
- SPI serial flash interface
- Support sleep and deep sleep mode for low power consumption
- Integrated high-fidelity stereo audio codec
  - Supports Line-in/out and mic-in/headset out
  - Differential mic input
  - 96dB SNR audio output
  - Optional digital interface (I^2S)
- Multiple external interfaces to adapt to various IoT and applications needs
  - 2 x UART
  - I^2C
  - 2 x low-speed, 10-bit ADCs
  - SPI
  - 11 x GPIO
- Clocks
  - Reference clock input 26MHz
  - Low power clock input at 32.768 kHz
  - 2 x clock outputs
  - Timers
  - 8 x 32-bit high speed timers
  - 4 timers with independent interrupts

Description

The ACH1190 is a single-chip host processor solution that is fully optimized for Audio and IoT applications. Built with ARM Cortex-M4, floating point, this host processor runs up to 200MHz (250 DMIPS), and is ideal for audio and video processing. It integrates 960K bytes of embedded SRAM for code and data execution. It also integrates a high-fidelity, 96dB SNR stereo audio codec for audio applications, with two fractional-N synthesizers to provide separate clock frequencies to CPU and audio codec to reduce audio interference. Equipped with various external interfaces, ACH1190 can be design in numerous types of host application scenarios. The ACH1190 also supports a crystal driver interface, thus able to generate reference clock to various wireless connectivity radio controllers, such as Wifi/Bluetooth/Zigbee.

With BGA and QFN package, it supports a high level of integration, compact and cost-effective designs, and delivers fast time-to-market.

Contents

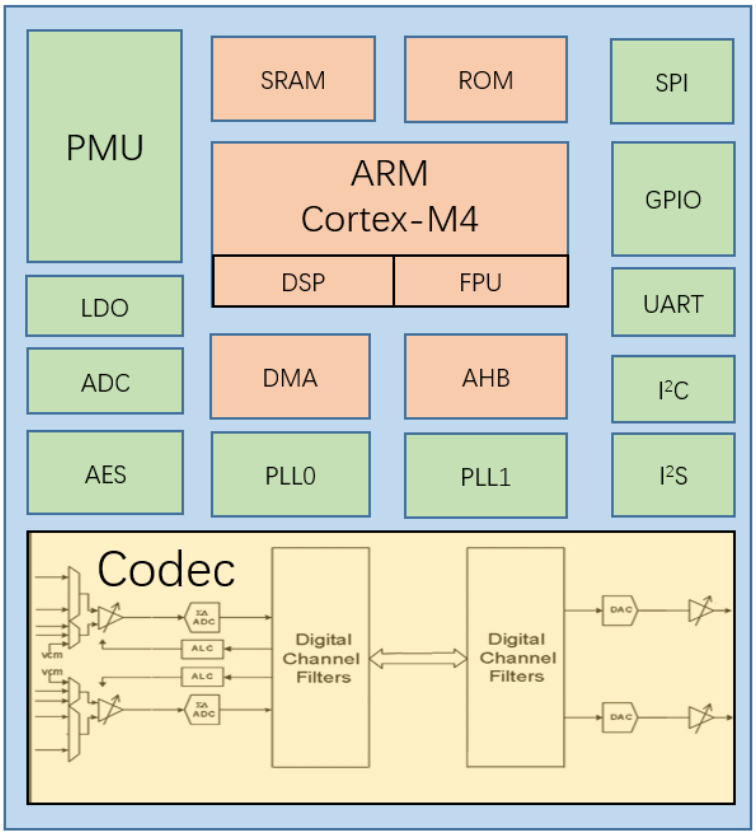
1. Introduction

The ACH1190 is a host processor single-chip solution, fully optimized for audio DSP and wireless host embedded applications featuring an ARM Cortex-M4 floating point processor. Integrating a high-fidelity stereo audio codec, it can support differential microphone inputs, headphone output, and Line-in/out. It also includes two fractional-N PLL blocks providing different high accuracy clocks, for the main CPU and audio codec – significantly reducing interference. The main CPU system can run up to 200MHz for intensive audio/video applications, audio DSP processing, and general purpose application hosting. The ACH1190 also comes with 960K byte internal run-time SRAM. With a variety of external interfaces, UART, SPI, I²C, I²S, ADCs, and GPIOs, it can be easily support designs for most applications with lower BOM and external component cost.

2. General Hardware Description

2.1. Block Diagram

Figure 1. ACH1190 internal block diagram



2.2. Pin functions

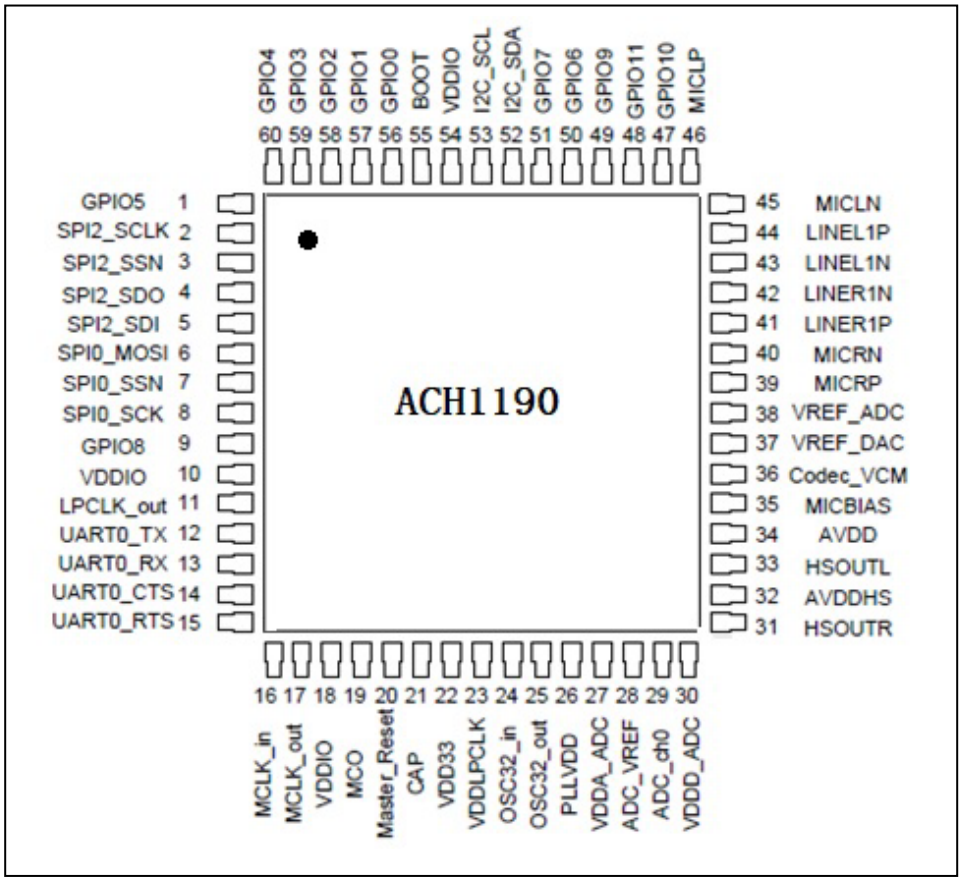
Table 1. ACH1190 functional and supply pin list QFN package

Pad	Name (Default)	Alternate usage ALT_0	Alternate usage ALT_1	Description
	Digital Signal			
6	SPI0_MOSI	UART1_CTS		RF Controller Interface
7	SPI0_NSS	UART1_RTS		
8	SPI0_SCK	UART1_TX		
9	SPI0_MISO	UART1_RX	GPIO_8	
12	UART0_TX			UART0
13	UART0_RX			
14	UART0_CTS			
15	UART0_RTS			
47	JTDI	UART2_RX	GPIO_10	JTAG
48	JTDO	UART2_TX	GPIO_11	
49	TRSTn	UART2_CTS	GPIO_9	
56	GPIO_0	UART2_RTS		
57	GPIO_1	I2S1_WS	SPI1_CS	GPIO
58	GPIO_2	I2S1_CK	SPI1_CLK	
59	GPIO_3	I2S1_RX	SPI1_MISO	
60	GPIO_4	I2S1_TX	SPI1_MOSI	
1	GPIO_5			
2	SPI2 SCK			SPI2 Serial NOR Flash
3	SPI2 SS			
4	SPI2 SDO			
5	SPI2 SDI			
50	TCK/SWCLK	GPIO_6		JTAG or User Interface
51	TMS/SWDIO	GPIO_7		
52	I2C0_SDA			I2C0
53	I2C0_SCL			
	Clock Signal			
24	OSC32_IN			32kHz crystal input
25	OSC32_OUT			32kHz crystal input (differential pair)
16	OSC_IN			26MHz crystal input
17	OSC_OUT			26MHz crystal input (differential pair)
19	MCO			Main PLL Clock output
11	CLK32K_OUT			32kHz buffer clock output
	Audio Signal			
46	MICIP_L			Microphone Input
45	MICIN_L			
39	MICIP_R			

40	MICIN_R			
44	LINE_L_1P			Line-In
43	LINE_L_1N			
42	LINE_R_1N			
41	LINE_R_1P			
31	RHPOUT			Headset Output (8 ohms)
33	LHPOUT			
	Control Signal			
20	RESET			Reset (Active Low)
55	BOOT			Test pin
	Analog Signal			
29	ADC0			10-bit ADC
	Reference Signal			
21	Vcap			
28	Vref_ADC			
38	Vref_AD			Codec Internally generated ADCs reference voltage pin for off-chip decoupling. Connect 1uF tantalum and 100nF ceramic capacitors to agndref.
37	Vref_DA			Codec Internally generated DACs reference voltage pin for off-chip decoupling. Connect 1uF tantalum and 100nF ceramic capacitors to agndref.
36	Codec_VCM			Codec Internally generated common-mode voltage pin for off-chip decoupling. Connect 10uF tantalum and 100nF ceramic capacitors to agnd.
35	MICBIAS			Microphone bias voltage output
	Power Supply			
30	VDDD_ADC			ADC Analog Supply
27	VDDA_ADC			ADC Digital Supply
32	AVDDHS			Codec Analog power supply for headset drivers. Connect 10uF tantalum and 100nF ceramic capacitors to AGND.
34	AVDD			Codec Analog power supply. Connect 10uF tantalum and 100nF ceramic capacitors to AGND.
26	PLLVDD			PLL Analog Supply
23	VDDLPCLK			PLL IO Supply
22	VDD33			Power supply (3.3V)
10	VDDIO			Digital IO Supply
18	VDDIO			
54	VDDIO			
	PAD			GND

2.3. Pinout Diagram

Figure 2. ACH1190 QFN60 pinout



3. Reset

3.1. Boot modes

An embedded BOOT ROM will run at startup.

When the BOOT PIN is low (0), the SPI 2 is used to load an 8K byte section of an external Flash memory into the internal RAM: loads 8K bytes from location 0x00000000 external Flash to location 0x20000000 internal RAM.

When the BOOT PIN is high (1), the UART 0 boot mode interface will become active. This interface allows data to be loaded from UART 0 into RAM using a set of boot commands. Note that these boot commands are generally used for testing and are not included in this document.

4. System Memory Map

Address	Peripheral
0x0000_0000 to 0x000F_FFFF	BOOT ROM
0x2000_0000 to 0x200F_EFFF	SRAM
0x4002 1800 – 0x4002 1FFF	SPI0
0x4002 2000 – 0x4002 27FF	SPI1
0x4002 2800 – 0x4002 2FFF	I2S0
0x4002 3000 – 0x4002 37FF	UART0
0x4002 3800 – 0x4002 3FFF	UART1
0x4002 4000 – 0x4002 47FF	I2S1 CODEC
0x4002 4800 – 0x4002 4FFF	SPI2 FLASH
0x4002 5000 – 0x4002 57FF	I2C0
0x4002 5800 – 0x4002 5FFF	CODEC
0x4002 6000 – 0x4002 67FF	UART2
0x4003 1800 – 0x4003 1FFF	GPIO
0x4003 3000 – 0x4003 37FF	WDT
0x4003 3800 – 0x4003 3FFF	ADC0
0x4003 4000 – 0x4003 47FF	ADC1
0x4003 4800 – 0x4003 4FFF	AES
0x4003 5800 – 0x4003 5FFF	SYSCFG
0x4003 6000 – 0x4003 67FF	TIMER

5. Serial Peripheral Interface, SPI

Three SPI ports are supported, usable in Master mode up to 40Mbps. Below is the feature list for the SPI devices:

- Data bus widths of 8, 16, and 32 bits.
- FIFO depth – Configurable depth of the transmit and receive FIFO buffers from 1 to 128 words deep.
- Programmable levels of FIFO interrupt for receive and transmit.
- Independent masking of interrupts – Master collision, transmit FIFO overflow, transmit FIFO empty, receive FIFO full, receive FIFO underflow, and receive FIFO overflow interrupts can all be masked independently.
- Multi-master contention detection – Informs the processor of multiple serial-master accesses on the serial bus.
- Programmable delay on the sample time of the received serial data bit (rxd), when configured in Master Mode; enables programmable control of routing delays resulting in higher serial data-bit rates.
- Serial interface operation – Choice of Motorola SPI, Texas Instruments Synchronous Serial Protocol or National Semiconductor Microwire.
- Clock bit-rate – Dynamic control of the serial bit rate of the data transfer.
- Hardware/software slave-select – Dedicated hardware slave-select lines can be used or software control can be used to target the serial-slave device.
- Serial clock polarity – This configuration option selects the serial-clock polarity of the SPI format directly after reset.
- Serial clock phase – This configuration option selects the serial-clock phase of the SPI format directly after reset.

5.1. SPI Register Definitions

Register	Offset	Size	Description
CTRLR0	0x00	21b	Control Register 0
CTRLR1	0x04	16b	Control Register 1
SSIENR	0x08	1b	SSI Enable
BAUDR	0x14	16b	Baud Rate Select
TXFTLR	0x18	6b	Transmit FIFO Threshold Level
RXFTLR	0x1C	6b	Receive FIFO Threshold Level
TXFLR	0x20	7b	Transmit FIFO Level
RXFLR	0x24	7b	Receive FIFO Level
SR	0x28	7b	Status
IMR	0x2C	6b	Interrupt Mask
ISR	0x30	6b	Interrupt Status
RISR	0x34	6b	Raw Interrupt Status
TXOICR	0x38	1b	Transmit FIFO Overflow Interrupt Clear
RXOCR	0x3C	1b	Receive FIFO Overflow Interrupt Clear
RXUICR	0x40	1b	Receive FIFO Underflow Interrupt Clear
MSTICR	0x44	1b	Multi-Master Interrupt Clear
ICR	0x48	1b	Interrupt Clear
DR	0x60	32b	Data

5.1.1 CTRLR0

Setting	Position	Description
DFS	0-3	Selects frame size in 16bit xfer mode. Data must be Right justified. Use: binary value +1. For example

		0x4 = 5-bit size, 0xF = 16-bit size.
FRF	4-5	Frame format. 00: Motorola SPI, 01: Texas Instruments SSP, 10 and 11: reserved.
SCPH	6	Clock phase, valid in Motorola SPI mode. 0: middle of first bit, 1: start of first bit.
SCPOL	7	Clock polarity, valid in Motorola SPI mode. 0: inactive low, 1: inactive high
Reserved	8-15	
DFS_32	16-20	Selects frame size in 32bit xfer mode. Data must be right justified. Use binary value +1. For example 0x1F = 32-bit size.
Reserved	21-31	

5.1.2 CTRLR1

Setting	Position	Description
NDF	0-15	Number of data frames. Receive data until the number of frames equals value +1. Maximum of 64KB data.

5.1.3 SSIENR

Setting	Position	Description
SSI_EN	0	When disable, all transfers are halted, transmit and receive FIFO buffers are cleared. Maybe be disabled for low power mode. 1: enable, 0: disable.

5.1.4 BAUDR

Setting	Position	Description
SCKDV	0-15	The frequency of the sclk is Fsclk = Fssi_clk/SCKDV

5.1.5 TXFTLR

Setting	Position	Description
TFT	0-6	Transmit FIFO Threshold. Level of entries, TFT value, (or below) at which the transmit FIFO controller triggers the tx empty interrupt: 0-127. For example: 0x0F will assert TXE when 15 or fewer data entries are present.

5.1.6 RXFTLR

Setting	Position	Description
RFT	0-6	Receive FIFO Threshold. Level of entries, RFT value +1, (or above) at which the receive FIFO controller triggers the RX full interrupt: 1-128. For example: 0x7F will assert RXF when 256 or more data entries are present.

5.1.7 TXFLR

Setting	Position	Description
TXTFL	0-7	Transmit FIFO Level. Number of data entries in the transmit FIFO, 0-128.

5.1.8 RXFLR

Setting	Position	Description
RFTFL	0-7	Receive FIFO Level. Number of data entries in the transmit FIFO, 0-128.

5.1.9 SR

Setting	Position	Description
Busy	0	SSI Busy Flag. When set, indicates that a transfer is in progress. When clear, indicates that the SPI is idle or disabled.
TFNF	1	Transmit FIFO Not Full. Set when the transmit FIFO contains one or more empty location, and is clear when the FIFO is full.
TFE	2	Transmit FIFO Empty. When the transmit FIFO is completely empty, this bit is set. Otherwise, is clear. This bit does not request an interrupt.
RFNE	3	Receive FIFO Not Empty. Set when the receive FIFO contains one or more entries, and is clear when the receive FIFO is empty. This bit can be polled to completely empty the FIFO.
RFF	4	Receive FIFO Full. When the receive FIFO is completely full, this bit is set. Otherwise, it is clear.
TXE	5	Transmission Error. Set if the transmit FIFO is empty when a transfer is started.
DCOL	6	Data Collision Error. This bit is set if the ss_in_n input is asserted by another master, while in the middle of a transfer. The data would be halted before completion.

5.1.10 IMR

Setting	Position	Description
TXEIM	0	Receive FIFO Empty Interrupt Mask. 0: TXE_INTR interrupt is masked, 1: interrupt is not masked.
TXOIM	1	Transmit FIFO Overflow Interrupt Mask. 0: TXO_INTR interrupt is masked, 1: interrupt is not masked.
RXUIM	2	Receive FIFO Underflow Interrupt Mask. 0: RXU_INTR interrupt is masked, 1: interrupt is not masked.
RXIOM	3	Receive FIFO Overflow Interrupt Mask. 0: RXO_INTR interrupt is masked, 1: interrupt is not masked.
RXFIM	4	Receive FIFO Full Interrupt Mask. 0: RXF_INTR interrupt is masked, 1: interrupt is not masked.
MSTIM	5	Multi-Master Contention Interrupt Mask. 0: MST_INTR interrupt masked, 1: interrupt is not masked.

5.1.11 ISR

Setting	Position	Description
TXEIS	0	Receive FIFO Empty Interrupt Status. 0: TXE_INTR interrupt is not active after masking, 1: interrupt is active after masking.
TXOIS	1	Transmit FIFO Overflow Interrupt Status. 0: TXO_INTR interrupt is not active after masking, 1: interrupt is active after masking.
RXUIS	2	Receive FIFO Underflow Interrupt Status. 0: RXU_INTR interrupt is not active after masking, 1: interrupt is active after masking.
RXIOS	3	Receive FIFO Overflow Interrupt Status. 0: RXO_INTR interrupt is not active after masking, 1: interrupt is active after masking.
RXFIS	4	Receive FIFO Full Interrupt Status. 0: RXF_INTR interrupt is not active after masking, 1: interrupt is active after masking.
MSTIS	5	Multi-Master Contention Interrupt Status. 0: MST_INTR interrupt not active after masking, 1: interrupt is active after masking.

5.1.12 RISR

Setting	Position	Description
TXEIR	0	Receive FIFO Empty Raw Interrupt Status. 0: TXE_INTR interrupt is not active prior to masking, 1: interrupt is active prior to masking.
TXOIR	1	Transmit FIFO Overflow Raw Interrupt Status. 0: TXO_INTR interrupt is not prior to after masking, 1: interrupt is active prior to masking.
RXUIR	2	Receive FIFO Underflow Raw Interrupt Status. 0: RXU_INTR interrupt is not active prior to masking, 1: interrupt is active prior to masking.
RXIOR	3	Receive FIFO Overflow Raw Interrupt Status. 0: RXO_INTR interrupt is not active prior to asking, 1: interrupt is active prior to masking.
RXFIR	4	Receive FIFO Full Raw Interrupt Status. 0: RXF_INTR interrupt is not prior to after asking, 1: interrupt is active prior to masking.
MSTIR	5	Multi-Master Contention Raw Interrupt Status. 0: MST_INTR interrupt not active prior to masking, 1: interrupt is active prior to masking.

5.1.13 TXOICR

Setting	Position	Description
TXOICR	0	Clear Transmit FIFO Overflow Interrupt. Reflects the status of the interrupt. A read from this register clears the TXO_INTR interrupt. Writing has no effect.

5.1.14 RXOICR

Setting	Position	Description
RXOICR	0	Clear Receive FIFO Overflow Interrupt. Reflects the status of the interrupt. A read from this register clears the RXO_INTR interrupt. Writing has no effect.

5.1.15 RXUICR

Setting	Position	Description
RXUICR	0	Clear Receive FIFO Underflow Interrupt. Reflects the status of the interrupt. A read from this register clears the RXU_INTR interrupt. Writing has no effect.

5.1.16 MSTICR

Setting	Position	Description
MSTICR	0	Clear Multi-Master Contention Interrupt. Reflects The status of the interrupt. A read from this Register clears the MST_INTR interrupt. Writing has no effect.

5.1.17 ICR

Setting	Position	Description
ICR	0	Clear Interrupts. This register is set if any of these interrupts are active: TXO_INTR, RXU_INTR, RXO_INTR, or MST_INTR. A read from this register clears these interrupts. Writing has no effect.

5.1.18 DR

Setting	Position	Description
DR	0-31	Data Read/Write. Size is 16 or 32 bits depending transfer size. The corresponding read or write FIFO is accessed when this register is read or written to.

6. Inter-integrated Sound, I²S

Two I2S ports supporting Master mode are available. One of these ports is routed to the internal integrated CODEC, and is not connectable to external pins. The other I2S port is for external peripheral access. Below are the features:

- I2S transmitter and/or receiver based on the Philips I²S serial protocol.
- Configurable number of stereo channels (up to 4) for both transmitter and receiver.
- Full duplex communication due to the independence of transmitter and receiver.
- Asynchronous clocking of APB bus and I2S sclk.
- Master mode of operation.
- Audio data resolutions of 12, 16, 20, 24, and 32 bits per sample.
- FIFO depth of 16 samples.
- Programmable FIFO thresholds.

6.1. I²S Register Definitions

Register	Offset	Size	Description
IER	0x00	1b	I2S Enable
IRER	0x04	1b	Receiver Block Enable
ITER	0x08	1b	Receiver Block Enable
CER	0x0C	1b	Clock Enable
CCR	0x10	5b	Clock Configuration
RXFFR	0x14	1b	Receive FIFO Reset
TXFFR	0x18	1b	Transmit FIFO Reset
CHANNEL_0	0x20		Channel 0
CHANNEL_1	0x60		Channel 1
CHANNEL_2	0XA0		Channel 2
CHANNEL_3	0xE0		Channel 3
COMP_2	0x1F0	32b	Component Parameter 2 Register
COMP_1	0x1F4	32b	Component Parameter 1 Register

6.1.1 IER

Setting	Position	Description
IEN	0	A disable on this bit will override any other block or channel enables and will flush the FIFOs. 1: enable, 0: disable.

6.1.2 IRER

Setting	Position	Description
RXEN	0	Receiver block enable. 1: enable, 0: disable.

6.1.3 ITER

Setting	Position	Description
TXEN	0	Transmitter block enable. 1: enable, 0: disable.

6.1.4 CER

Setting	Position	Description
CLKEN	0	Clock generation enable/disable. 1: clock generation enable, 0: clock generation disable

6.1.5 CCR

Setting	Position	Description
SCLKG	0-2	Clock gating setting: 0: No clock gating 1: Gate after 12 clock cycles 2: Gate after 16 clock cycles 3: Gate after 20 clock cycles 4: Gate after 24 clock cycles This value should be greater than or equal to the largest configured audio resolution to prevent truncating RX/TX audio data.
WSS	3-4	Cycles for which word select line, ws_out, stays In the left or right sample mode: 0: 16 clock cycles

		1: 24 clock cycles 2: 32 clock cycles The clock generation block must be disabled prior to any changes in this value.

6.1.6 RXFFR

Setting	Position	Description
RXFFR	0	Receive FIFO Reset. Writing a 1 to this register flushes all the RX FIFOs. This bit will self-clear.

6.1.7 TXFFR

Setting	Position	Description
TXFFR	0	Transmitter FIFO Reset. Writing a 1 to this register flushes all the TX FIFOs. This bit will self-clear.

6.1.8 COMP_2

Setting	Position	Description
RX_WSIZE_0	0-2	0: 12 bit resolution
RX_WSIZE_1	3-5	1: 16 bit resolution
Reserved	6	2: 20 bit resolution
RX_WSIZE_2	7-9	3: 24 bit resolution
RX_WSIZE_3	10-12	4: 32 bit resolution 5-7: reserved

6.1.9 COMP_1

Setting	Position	Description
APB_WIDTH 0-1		0: 8 bits, 1: 16 bits, 2: 32 bits
FIFO_DEPTH	2-3	0: 2 words, 1: 4 words, 2: 8 words, 3: 16 words
MODE_EN	4	0: disable, 1: enable
TX_BLOCK	5	0: disable, 1: enable
RX_BLOCK	6	0: disable, 1: enable
RX_CHANNELS	7-8	0-3: 1-4 channels
TX_CHANNELS	9-10	0-3: 1-4 channels
Reserved	11-15	
TX_WSIZE_0	16-18	0: 12 bit resolution
TX_WSIZE_1	19-21	1: 16 bit resolution
TX_WSIZE_2	22-24	2: 20 bit resolution
TX_WSIZE_3	25-27	3: 24 bit resolution 4: 32 bit resolution

6.1.10 CHANNEL_X

6.1.10.1. LRBRx offset 0x00 size 32b Left Receive Buffer

Setting	Position	Description
RX_WORD	0-31	Right justified RX data for left channel

6.1.10.2. LTHRx offset 0x00 size 32b Left Transmit Holding

Setting	Position	Description
TX_WORD	0-31	Right justified TX data for left channel

6.1.10.3. RRBRx offset 0x04 size 32b Left Receive Buffer

Setting	Position	Description
RX_WORD	0-31	Right justified RX data for right channel

6.1.10.4. RTHRx offset 0x04 size 32b Left Transmit Holding

Setting	Position	Description
TX_WORD	0-31	Right justified TX data for right channel

6.1.10.5. RERx offset 0x08 size 1b Receive Enable

Setting	Position	Description
RXCHEN	0	Receive channel enable. Begins receiving on the next stereo cycle. 0: disable, 1: enable

6.1.10.6. TERx offset 0x0C size 1b Transmit Enable

Setting	Position	Description
TXCHEN	0	Transmit channel enable. Begins transmitting on the next stereo cycle. 0: disable, 1: enable

6.1.10.7. RCRx offset 0x10 size 3b Receive Configuration

Setting	Position	Description
WLEN	0-2	Resolution of the receiver. Channel must be disabled to change this setting. 0x0: ignore word length 0x1: 12 bit resolution 0x2: 16 bit resolution 0x3: 20 bit resolution 0x4: 24 bit resolution 0x5: 32 bit resolution

6.1.10.8. TCRx offset 0x14 size 3b Transmit Configuration

Setting	Position	Description
WLEN	0-2	Resolution of the transmitter. Channel must be disabled to change this setting. 0x0: ignore word length 0x1: 12 bit resolution 0x2: 16 bit resolution 0x3: 20 bit resolution 0x4: 24 bit resolution 0x5: 32 bit resolution

6.1.10.9. ISRx offset 0x18 size 6b Interrupt Status

Setting	Position	Description
RXDA	0	Status or Receive Data Available Interrupt. RX FIFO data available. 0: trigger level not reached, 1: trigger level reached.
RXFO	1	Status or RX channel Data Overrun. Incoming data lost due to full FIFO. 0: RX FIFO valid, 1: RX FIFO overrun.
Reserved	2-3	
TXFE	4	Status of Transmit Empty Trigger Interrupt. TX FIFO is empty. 0: trigger level not reached, 1: Trigger level reached.

TXFO	5	Status of TX channel Data Overrun. Attempt to write To full TX FIFO. 0: TX FIFO write valid, 1: TX FIFO write overrun.

6.1.10.10. IMRx offset 0x1C size 6b Interrupt Mask

Setting	Position	Description
RXDAM	0	Mask RX FIFO Data Available Interrupt. 0: unmask interrupt 1: mask interrupt
RXFOM	1	Mask RX FIFO Overrun Interrupt. 0: unmask interrupt 1: mask interrupt
Reserved	2-3	
TXFEM	4	Mask TX FIFO Data Empty Interrupt. 0: unmask interrupt 1: mask interrupt
TXFOM	5	Mask TX FIFO Overrun Interrupt. 0: unmask interrupt 1: mask interrupt

6.1.10.11. RORx offset 0x20 size 1b Receive Overrun

Setting	Position	Description
RXCHO	0	Read this bit to clear RX FIFO Data Overrun. 0: RX FIFO valid 1: RX FIFO overrun

6.1.10.12. TORx offset 0x24 size 1b Transmit Overrun

Setting	Position	Description
TXCHO	0	Read this bit to clear TX FIFO Data Overrun. 0: TX FIFO valid 1: TX FIFO overrun

6.1.10.13. RFCRx offset 0x28 size 4b Receive FIFO Configure

Setting	Position	Description
RXCHDT	0-3	Set the trigger level of the RX FIFO at which the Received Data Available interrupt is triggered. Trigger Level = RXCHDT value + 1, from 1-16.

6.1.10.14. TFCRx offset 0x2C size 4b Transmit FIFO Configure

Setting	Position	Description
TXCHET	0-3	Set the trigger level of the TX FIFO at which the Empty Threshold Reached interrupt is triggered. Trigger Level = TXCHDT value, from 0-15.

6.1.10.15. RFFx offset 0x30 size 1b Receive FIFO Flush

Setting	Position	Description
RXCHFR	0	RX channel FIFO reset. Write a 1 to this bit to flush the RX FIFO. This will self-clear. RX channel must be disabled prior to writing.

6.1.10.16. TFFx offset 0x34 size 1b TransmiT FIFO Flush

Setting	Position	Description
RXCHFR	0	TX channel FIFO reset. Write a 1 to this bit to

flush the TX FIFO. This will self-clear. TX channel must be disabled or blocked prior to writing.

7. Two-wire Interface, I²C

One I2C port is available, supporting two-wire interface. Below are the features:

- Serial data line, SDA, and serial clock, CLK.
- Two speeds:
  - Standard <100 Kb/s
  - Fast 400 Kb/s
- Clock synchronization
- Master or slave I²C operation
- 7 or 10 bit addressing
- 7 or 10 bit combined format transfers
- Bulk transmit mode
- TX and RX buffers
- Interrupt or polled operation
- Handles bit and byte waiting

7.1. I²C Register Definitions

Register	Offset	Size	Description
CON	0x00	10b	I²C Control
TAR	0x04	13b	I²C Target Address
SAR	0x08	10b	I²C Slave Address
DATA_CMD	0x10	12b	RX/TX Buffer and Command
SS_SCL_HCNT	0x14	16b	Standard Speed Clock High Count
SS_SCL_LCNT	0x18	16b	Standard Speed Clock Low Count
FS_SCL_HCNT	0x1C	16b	Fast Mode Clock High Count
FS_SCL_LCNT	0x20	16b	Fast Mode Clock Low Count
INTR_STAT	0x2C	14b	Interrupt Status
INTR_MASK	0x30	14b	Interrupt Mask
RAW_INTR_STAT	0x34	14b	Raw Interrupt Status
RX_TL	0x38	3b	Receive FIFO Threshold
TX_TL	0x3C	3b	Transmit FIFO Threshold
CLR_INTR	0x40	1b	Clear Combined and Individual Interrupt
CLR_RX_UNDER	0x44	1b	Clear RX_UNDER Interrupt
CLR_RX_OVER	0x48	1b	Clear RX_OVER Interrupt
CLR_TX_OVER	0x4C	1b	Clear TX_OVER Interrupt
CLR_RD_REQ	0x50	1b	Clear RD_REQ Interrupt
CLR_TX_ABRT	0x54	1b	Clear TX_ABRT Interrupt
CLR_RX_DONE	0x58	1b	Clear RX_DONE Interrupt
CLR_ACTIVITY	0x5C	1b	Clear ACTIVITY Interrupt
CLR_STOP_DET	0x60	1b	Clear STOP_DET Interrupt
CLR_START_DET	0x64	1b	Clear START_DET Interrupt
CLR_GEN_CALL	0x68	1b	Clear GEN_CALL Interrupt
ENABLE	0x6C	3b	I²C Enable
STATUS	0x70	11b	Status
TXFLR	0x74	3b	Transmit FIFO Level
RXFLR	0x78	3b	Receive FIFO Level
SDA_HOLD	0x7C	24b	SDA Hold Time Length
TX_ABRT_SOURCE	0x80	32b	Transmit Abort Status
SLV_DATA_NACK_ONLY	0x84	1b	Generate SLV_DATA_NACK
SDA_SETUP	0x94	8b	SDA Setup

ACK_GENERAL_CALL	0x98	1b	ACK General Call
ENABLE_STATUS	0x9C	3b	Enable Status
CLR_RESTART_DET	0xA8	1b	Clear RESTART_DET Interrupt

7.1.1 CON

Setting	Position	Description
MASTER_MODE	0	This bit controls whether the I2C master is enabled. 1: enable, 0: disable.
SPEED	1-2	Speed of I2C operation, when master. 1: standard mode, 2: fast mode, 3: reserved
SADDR_SIZE	3	As a slave, sets either 7 or 10 bit address size. 0: 7 bit, 1: 10 bit
MADDR_SIZE	4	As a master, sets either 7 or 10 bit address size. 0: 7 bit, 1: 10 bit
RESTART_EN	5	As a master, determines if RESTART conditions are sent: sending a START BYTE, direction changes, read operation with 10 bit address. 0: disable, 1: enable
SLAVE_DIS	6	Disables the slave operation, must be set to 1 after reset to disable. 0: enable (default) 1: disable
STP_DET_ADDR	7	In slave mode, 0: issues STOP_DET irrespective of whether it's addressed or not, 1: issues STOP_DET interrupt only when it is addressed.
EMPTY_CTRL	8	TX_EMPTY interrupt generated when set to 1.
FULL_HLD_CNT	9	Holds the bus when the RX FIFO is full to the buffer Depth when set to 1.
STP_DET_MAST	10	In master mode, 0: issues STOP_DET irrespective of Whether the master is active, 1: issues the STOP_DET interrupt only when the master is active.

7.1.2 TAR

Setting	Position	Description
TAR	0-9	Target address for any master transaction. Ignored during a General Call.
GC_OR_START	10	If bit 11, SPECIAL, is set to 1, then this bit indicates whether a General Call or START byte is performed. 0: General Call Address – after issuing a General Call, only writes may be performed. I2C remains in General Call mode until SPECIAL bit is cleared, 1: START BYTE.
SPECIAL	11	Performs General Call or START BYTE command. 0: ignore bit 10 and use TAR normally, 1: perform Special I2C command as specified in bit 10.
10BIT_MAST	12	As a master, starts transfers in 7 or 10 bit mode, 0: 7 bit, 1: 10 bit

7.1.3 SAR

Setting	Position	Description
SAR	0-9	Target address for slave.

7.1.4 DATA_CMD

Setting	Position	Description
DAT	0-7	Contains the data to be transmitted or receive on the I2C bus.
CMD	8	Determines if read or write is performed when in master mode. 0: Write, 1: Read.
STOP	9	Controls whether a STOP is issued after the byte is sent or received. Only available when EMPTYFIFO_HLD_MAST_EN is configured to 1. 0: STOP is not issued after this byte, regardless of whether or not the TX FIFO is empty, 1: STOP is issued after this byte, regardless of whether or not the TX FIFO is empty.
RESTART	10	Controls whether a RESTART is issued before the byte is sent/received. Only available when EMPTYFIFO_HLD_MAST_EN is configured to 1. 0: if RESTART_EN is a 1, RESTART is issued only if the transfer direction is changing from the previous Command, 1: a RESTART is issued before the data is Sent/received regardless of whether or not the transfer direction is changing.
FIRST_BYTE	11	Indicates the first data byte received after the Address phase for receive transfer in Master or Slave receiver mode. Available when FIRST_DATA_BYTE_STATUS is set to 1.

7.1.5 SS_SCL_HCNT

Setting	Position	Description
SS_SCL_HCNT	0-15	Must be set before transactions can take place. Sets the SCL clock high-period count for standard speed. Can be written only when ENABLE is set to 0. Minimum value is 6.

7.1.6 SS_SCL_LCNT

Setting	Position	Description
SS_SCL_HCNT	0-15	Must be set before transactions can take place. Sets the SCL clock low-period count for standard speed. Can be written only when ENABLE is set to 0. Minimum value is 8.

7.1.7 FS_SCL_HCNT

Setting	Position	Description
SS_SCL_HCNT	0-15	Must be set before transactions can take place. Sets the SCL clock high-period count for fast mode. Can be written only when ENABLE is set to 0. Minimum value is 6.

7.1.8 FS_SCL_LCNT

Setting	Position	Description
SS_SCL_HCNT	0-15	Must be set before transactions can take place. Sets

		the SCL clock low-period count for fast mode. Can be written only when ENABLE is set to 0. Minimum value is 8.

7.1.9 INTR_STAT

Setting	Position	Description
RX_UNDER	0	Indicates the status of these interrupts.
RX_OVER	1	
RX_FULL	2	
TX_OVER	3	
TX_EMPTY	4	
RD_REQ	5	
TX_ABRT	6	
RX_DONE	7	
ACTIVITY	8	
STOP_DET	9	
START_DET	10	
GEN_CALL	11	
RESTART_DET	12	
MST_ON_HOLD	13	

7.1.10 INTR_MASK

Setting	Position	Description
RX_UNDER	0	These bits mask the corresponding interrupt status bits in the INTR_STAT register.
RX_OVER	1	
RX_FULL	2	
TX_OVER	3	
TX_EMPTY	4	
RD_REQ	5	
TX_ABRT	6	
RX_DONE	7	
ACTIVITY	8	
STOP_DET	9	
START_DET	10	
GEN_CALL	11	
RESTART_DET	12	
MST_ON_HOLD	13	

7.1.11 RAW_INTR_STAT

Setting	Position	Description
RX_UNDER	0	
RX_OVER	1	
RX_FULL	2	
TX_OVER	3	
TX_EMPTY	4	
RD_REQ	5	
TX_ABRT	6	
RX_DONE	7	
ACTIVITY	8	
STOP_DET	9	
START_DET	10	
GEN_CALL	11	

RESTART_DET	12
MST_ON_HOLD	13

7.1.12 RX_TL

Setting	Position	Description
RX_TL	0-2	Sets the level of entries or above, that triggers the RX_FULL interrupt. Threshold = entry value + 1.

7.1.13 TX_TL

Setting	Position	Description
TX_TL	0-2	Sets the level of entries or below, that triggers the TX_EMPTY interrupt. Range is 0-7.

7.1.14 CLR_INTR

Setting	Position	Description
CLR_INTR	0	Read this register to clear the combined, all Individual, and TX_ABRT_SOURCE interrupts.

7.1.15 CLR_RX_UNDER

Setting	Position	Description
CLR_RX_UNDER	0	Read this register to clear RX_UNDER.

7.1.16 CLR_RX_OVER

Setting	Position	Description
CLR_RX_OVER	0	Read this register to clear RX_OVER.

7.1.17 CLR_RD_REQ

Setting	Position	Description
CLR_RD_REQ	0	Read this register to clear RD_REQ.

7.1.18 CLR_TX_ABRT

Setting	Position	Description
CLR_TX_ABRT	0	Read this register to clear TX_ABRT.

7.1.19 CLR_RX_DONE

Setting	Position	Description
CLR_RX_DONE	0	Read this register to clear RX_DONE.

7.1.20 CLR_ACTIVITY

Setting	Position	Description
CLR_ACTIVITY	0	Read this register to clear ACTIVITY interrupt.

7.1.21 CLR_STOP_DET

Setting	Position	Description
CLR_ACTIVITY	0	Read this register to clear STOP_DET interrupt.

7.1.22 CLR_START_DET

Setting	Position	Description
CLR_ACTIVITY	0	Read this register to clear START_DET interrupt.

7.1.23 CLR_GEN_CALL

Setting	Position	Description
CLR_ACTIVITY	0	Read this register to clear GEN_CALL interrupt.

7.1.24 IC_ENABLE

Setting	Position	Description
ENABLE	0	Enables the I2C interface when set to 1. Before disabling, must flush the TX/RX FIFO.
ABORT	1	When set to 1, aborts the transfer: issues a STOP and flushes the TX FIFO after the current transfer is complete. This bit is cleared automatically.
TX_CMD_BLOCK	2	In Master mode, blocks the transmission of data when set to 1. When set to 0, starts transmission of data when available in the TX FIFO.

7.1.25 IC_STATUS

Setting	Position	Description
ACTIVITY	0	I^2C Activity Status
TFNF	1	TX FIFO contains one or more empty locations when set to 1.
TFE	2	TX FIFO is completely empty when set to 1.
RFNE	3	RX FIFO contains one or more entries when set to 1.
RFF	4	RX FIFO is completely full when set to 1.
MST_ACTIVITY	5	When Master is not in IDLE, this bit is set to 1.
SLV_ACTIVITY	6	When Slave is not in IDLE, this bit is set to 1.
MST_HOLD_TXE	7	If EMPTY_HOLD_MASTER_EN is set to 1, this will stall The write transfer when TX FIFO is empty, and the last byte does not have the STOP bit set.
MST_HOLD_RXF	8	Indicates the BUS hold in Master mode due to RX FIFO is full and additional data has been received.
SLV_HOLD_TXE	9	Indicates the BUS hold in Slave mode for the read request when the TX FIFO is empty. The bus is in hold until the TX FIFO has data to transmit for the read request.
SLV_HOLD_RXF	10	Indicates the BUS hold in Slave mode due to RX FIFO being full and additional data received.

7.1.26 TXFLR

Setting	Position	Description
TXFLR	0-2	Contains the number of valid entries in the TX FIFO.

7.1.27 RXFLR

Setting	Position	Description
RXFLR	0-2	Contains the number of valid entries in the RX FIFO.

7.1.28 SDA_HOLD

Setting	Position	Description
SDA_TX_HOLD	0-15	Sets the required SDA hold time in clock periods as a transmitter.
SDA_RX_HOLD	15-23	Sets the required SDA hold time in clock periods as a receiver.

7.1.29 ABRT_SOURCE

Setting	Position	Description
ABRT7B_ADDR_NK	0	Master in 7-bit address mode, address was not acked by any slave.
ABRT10B_ADDR1_NK	1	Master in 10-bit address mode, first 10-bit address byte was not acked by any slave. by any slave.
ABRT10B_ADDR2_NK	2	Master in 10-bit address mode, second 10-bit address byte was not acked by any slave.
ABRT_TXDATA_NK	3	Master transmission did not receive an ack from slave.
ABRT_GCALL_NK	4	Master mode sends a General Call and no slave acked.
Reserved	5-6	
ABRT_START_ACK	7	Master sends a START byte and the slave incorrectly acked this byte.
Reserved	8-22	
TX_FLUSH_CNT	23-21	Number of TX FIFO data commands that are flushed due to TX_ABRT interrupt. Cleared with I^2C is disabled.

7.1.30 SLV_DATA_NACK_ONLY

Setting	Position	Description
NACK	0	Generate NACK as a slave when set to 1. When set to 0, a NACK or ACK is generated normally.

7.1.31 SDA_SETUP

Setting	Position	Description
SDA_SETUP	0-7	SDA Setup. Number of clock periods introduced in the rising edge of the SCL, relative to SDA changing, by holding SCL low when the I^2C services a read request while a slave-transmitter. Minimum is 2; default is 0x64.

7.1.32 ACK_GENERAL_CALL

Setting	Position	Description
ACK_GEN_CALL	0	Ack General Call. When set to 1, the I^2C responds with an ACK when it receives a General Call. When set to 0, the I^2C does not generate General Call interrupts.

7.1.33 ENABLE_STATUS

Setting	Position	Description
EN	0	I2C Enable Status. When a 1, I²C is in enabled state. When a 0, I²C is inactive.
SLV_DIS_BUSY	1	Slave Disabled While Busy. This bit indicates if a potential or active slave operation has been aborted due to setting bit 0 in the ENABLE register from 1 to 0.
SLV_RX_LOST	2	Slave Received Data Lost. Indicates when a slave-receiver operation has been aborted with at least one data byte received.

7.1.34 CLR_RESTART_DET

Setting	Position	Description
CLR_RESTART_DET	0	Read this bit to clear the RESTART_DET interrupt.

8. UART Interface

Up to 3 UART ports (UART0, 1 and 2) are available in the ACH. Control registers are mapped to the APB bus. The following features are supported:

- Transmit and Receive FIFO of 256 Bytes
- Support industry-standard 16550
- Auto Flow Control with RTS/CTS hardware pin
- Programmable interrupts for Tx and Rx FIFO
- Programmable fractional baud rate support

8.1. UART Register Definition

Register	Offset	Size	Description
RBR	0x00	9b	Receive Buffer Register
THR	0x00	9b	Transmit Holding Register
DLL	0x00	8b	Divisor Latch (Low)
DLH	0x04	8b	Divisor Latch (High)
IER	0x04	8b	Interrupt Enable Register
IIR	0x08	8b	Interrupt Identification Register
FCR	0x08	8b	FIFO Control Register
LCR	0x0C	8b	Line Control Register
MCR	0x10	6b	Modem Control Register
LSR	0x14	9b	Line Status Register
MSR	0x18	8b	Modem Status Register
FAR	0x70	1b	FIFO Access Register
TFR	0x74	8b	Transmit FIFO Read
RFW	0x78	10b	Receive FIFO Write
USR	0x7C	5b	UART Status Register
TFL	0x80	9b	Transmit FIFO Level
RFL	0x84	9b	Receive FIFO Level
SRR	0x88	3b	Software Reset Register
DLF	0xC0	4b	Divisor Latch Fractional Value.

8.1.1 RBR

Setting	Position	Description

RX	0-7	Receive Buffer Register (LSB 8 bit)
RX	8	Receive Buffer Register (MSB 9th Bit)

8.1.2 THR

Setting	Position	Description
TX Register	0-7	Transmit Hold Register (LSB 8 bit)
TX Register	8	Transmit Hold Register (MSB 9th Bit)

8.1.3 DLL

Setting	Position	Description
DIV_LATCH	0-7	Lower 8 bits of a 16-bit, read/write, Divisor Latch register that contains the baud rate divisor for the UART.

8.1.4 DLH

Setting	Position	Description
DIV_LATCH	0-7	Upper 8 bits of a 16-bit, read/write, Divisor Latch register that contains the baud rate divisor for the UART.

8.1.5 IER

Setting	Position	Description
ERBFI	0	Enable Received Data Available Interrupt. 0: disable 1: enable
ETBEI	1	Enable Transmit Holding Register Empty Interrupt 0: disable 1: enable
ELSI	2	Enable Receiver Line Status Interrupt 0: disable 1: enable
EDSSI	3	Enable Modem Status Interrupt 0: disable 1: enable
Reserved	4-6	
PTIME	7	Programmable THRE Interrupt Mode Enable 0: disable 1: enable

8.1.6 IIR

Setting	Position	Description
INTR_ID	0-3	Interrupt ID. This indicates the highest priority pending interrupt which can be one of the following types: 0000: modem status 0001: no interrupt pending 0010: THR empty 0100: received data available 0110: receiver line status

		0111: busy detect 1100: character timeout
Reserved	4-5	
FIFOSE	6-7	FIFOs Enabled 0: disable 1: enable

8.1.7 FCR

Setting	Position	Description
FIFOE	0	FIFO Enable
RFIFOR	1	Receive FIFO Reset
XFIFOR	2	XMIT FIFO Reset
Reserved	3	
TET	4-5	TX Empty Trigger
RT	6-7	RCVR Trigger

8.1.8 LCR

Setting	Position	Description
DLS	0-1	Data Length Select. The number of bits that may be selected are as follows: 00: 5 bits 01: 6 bits 10: 7 bits 11: 8 bits
STOP	2	Number of Stop Bits 0: 1 stop bit 1: 1.5 stop bits when DLS is 0, else 2 stop bit
PEN	3	Parity Enable 0: disabled 1: enabled
EPS	4	Even parity select
STICK_PARITY	5	Stick Parity 0: disabled 1: enabled
BC	6	Break Control Bit. Causes a break on the receiving device when set to 1
DLAB	7	Divisor Latch Access Bit

8.1.9 MCR

Setting	Position	Description
DTR	0	Data Terminal Ready
RTS	1	Request to Send
Reserved	2-3	
LB	4	Loop Back Bit
AFCE	5	Auto Flow Control Enable 0: Auto Flow Control Mode disabled 1: Auto Flow Control Mode enabled

8.1.10 LSR

Setting	Position	Description
DR	0	Data Ready Bit 0: no data ready 1: data ready
OE	1	Overrun error bit 0: no overrun error 1: overrun error
PE	2	Parity error bit 0: no parity error 1: parity error
FE	3	Framing error bit 0: no framing error 1: framing error
BI	4	Break interrupt bit
THRE	5	Transmit Holding Register Empty bit
TEMT	6	Transmitter Empty bit.
RFE	7	Receive FIFO error bit 0: no error in RX FIFO 1: error in RX FIFO
ADDR_RCVD	8	Address Received bit 0: Indicates that the character is data. 1: Indicates that the character is an address.

8.1.11 MSR

Setting	Position	Description
DTCS	0	Delta Clear to Send 0: no change on CTS since last read of MSR 1: change on CTS since last read of MSR
DDSR	1	Delta Data Set Ready. 0: no change on DSR since last read of MSR 1: change on DSR since last read of MSR
TERI	2	Trailing Edge of Ring Indicator. 0: no change on RI since last read of MSR 1: change on RI since last read of MSR
DDCD	3	Delta Data Carrier Det 0: no change on DCD since last read of MSR 1: change on DCD since last read of MSR
CTS	4	Clear to Send 0: CTS input is de-asserted (logic 1) 1: CTS input is asserted (logic 0)
DSR	5	Data Set Ready 0: DSR input is de-asserted (logic 1) 1: DSR input is asserted (logic 0)
RI	6	Ring Indicator 0: RI input is de-asserted (logic 1) 1: RI input is asserted (logic 0)
DCD	7	Data Carrier Detect 0: DCD input is de-asserted (logic 1) 1: DCD input is asserted (logic 0)

8.1.12 FAR

Setting	Position	Description

FIFO_ACCESS	0	FIFO access mode. 0: FIFO access mode disabled 1: FIFO access mode enabled

8.1.13 TFR

Setting	Position	Description
TX_FIFO_RD	0-7	Read the data at the top of the transmit FIFO. Each read pops the TX FIFO and gives the next data value which was moved to the top of the FIFO.

8.1.14 RFW

Setting	Position	Description
RFWD	0-7	Data written to the RFWD is pushed to the RX FIFO. Each write pushes new data to the next write location in the RX FIFO.
RFPE	8	RX FIFO Parity Error.
RFFE	9	RX FIFO Framing Error.

8.1.15 USR

Setting	Position	Description
BUSY	0	UART Busy 0: UART is idle or inactive 1: UART is busy (transferring data)
TFNF	1	Transmit FIFO not full. 0: Transmit FIFO is full 1: Transmit FIFO is not full
TFE	2	Transmit FIFO Empty 0: Transmit FIFO is not empty 1: Transmit FIFO is empty
RFNE	3	Receive FIFO Not Empty 0: Receive FIFO is empty 1: Receive FIFO is not empty
RFF	4	Receive FIFO full. 0: Receive FIFO not full 1: Receive FIFO full

8.1.16 TFL

Setting	Position	Description
TXFIFO	0-8	TX FIFO Level

8.1.17 RFL

Setting	Position	Description
RXFIFO	0-8	RX FIFO Level

8.1.18 SRR

Setting	Position	Description
UR	0	UART reset

RFR	1	RCVR FIFO Reset
XFR	2	XMIT FIFO Reset

8.1.19 DLF

Setting	Position	Description
DLF	0-3	Fractional part of divisor

Value	Fraction	Fractional Value
0000	0/16	0.0000
0001	1/16	0.0625
0010	2/16	0.125
0011	3/16	0.1875
0100	4/16	0.25
0101	5/16	0.3125
0110	6/16	0.375
0111	7/16	0.4375
1000	8/16	0.5
1001	9/16	0.5625
1010	10/16	0.625
1011	11/16	0.6875
1100	12/16	0.75
1101	13/16	0.8125
1110	14/16	0.875
1111	15/16	0.9375

9. Audio CODEC

An integrated audio CODEC is available in the ACH. Control registers are mapped to the APB bus. Audio data is sent using a dedicated I²S port. The following features are supported:

- 24-bit D/A and A/D conversion.
- 90dB Dynamic Range and -80dB THD A/D Conversion.
- 96dB Dynamic Range and -86dB THD D/A Conversion.
- 2 Stereo Single-Ended/Differential Line-in and Microphones inputs.
- 1 Stereo Single-Ended Headset Driver.
- Built-in Microphone Bias.
- Built-in References and Biasing Circuitry.
- Analogue and Digital Gain with Soft-ramp Control.
- Input Automatic Volume Control (ALC).
- Power-on/off Pop-Suppression.
- Supported Audio Sampling Rates from 8 to 192 kHz.
- LPC standard I2S audio data interface in Master and Slave Mode Operation.

10. Clock specifications

The ACH1190 uses two clocks: a reference clock and an optional low power clock. For the reference clock, the ACH1190 can either use an external reference clock source or generate its own reference using a XTAL. The low-power clock must always be supplied from an external source.

Table 2. Main crystal specifications

Symbol	Parameter	Min	Typ	Max	Unit
External crystal					
F_{IN}	Clock input frequency list		26		MHz

F_{INTOL}	Tolerance on input frequency (typical)	-20	-	+20	ppm

Table 3. Low power clock specifications

Symbol	Parameter	Min	Typ	Max	Unit
F_{IN}	Clock input frequencies		32.768		kHz
F_{INTOL}	Tolerance on input frequency	-1000	-	+1000	ppm

11.AHB Bus Matrix

The 32-bit multi-AHB bus matrix interconnects all the masters (CPU and DMA) and slaves APB peripherals and ensures an efficient seamless operation even when several high-speed peripherals work simultaneously.

12. Embedded SRAM

Up to 960K bytes of system SRAM available for code and data RAM. RAM memory is accessed (read/write) at CPU clock speed. It can be enable/disable through clock gating to reduce the power consumption.

13.Electrical Characteristics

13.1. Absolute maximum ratings

The Absolute Maximum Rating (AMR) corresponds to the maximum value that can be applied without leading to instantaneous or very short-term unrecoverable hard failure (destructive breakdown).

Table 4. Absolute maximum ratings

Symbol	Parameter	Min	Max	Unit
V_{DD}	Digital Supply voltages	-0.3	+3.3	V
V_{CCA_PLL}	Analog PLL Supply voltage	-0.3	+3.6	V
V_{CC_HP}	Supply voltage I/O	-0.3	+3.6	V
$V_{CCA\_MAIN\_PLL}$	Supply voltage I/O	-0.3	+3.6	V
V_{in}	Input voltage on any digital pin	-0.3	+3.3	V
V_{ssdiff}	Maximum voltage difference between different types of Vss pins	-0.3	+0.3	V
T_{stg}	Storage temperature	-65	+100	°C

13.2. Operating ranges

Operating ranges define the limits for functional operation and parametric characteristics of the device. Functionality outside these limits is not guaranteed.

Table 5. Operating ranges

Symbol	Parameter	Min	Typ	Max	Unit
T_{amb}	Operating ambient temperature	-30	+25	+70	°C
V_{DD}	Digital Supply Voltage	+1.8	+2.5	+3.3	V

V_{CCA_PLL}	Analog Audio PLL Supply Voltage	+1.8	+2.5	+3.6	V
V_{CC_HP}	Analog Headset Supply Voltage	+2.5	+3.3	+3.6	V
$V_{CCA\_MAIN\_PLL}$	Analog Main PLL Supply Voltage	+1.8	+3.3	+3.6	V

13.3. Digital I/O specifications

All I/Os, except analog I/Os or otherwise specified are standard I/Os with levels complying with the EIA/JEDEC standard JESD8-7.

Table 6. DC and AC input specifications

Symbol	Parameter	Min	Typ	Max	Unit
Input levels					
V_{IL}	Low-level input voltage	0	-	0.35 * V_{DD_IO}	V
V_{IH}	High-level input voltage	0.65 * V_{DD_IO}	-	-	V
V_{hyst}	Schmitt trigger hysteresis	150	-	-	mV
T_r/T_f	Rise and fall time that can be present on inputs	-	-	25	ns
R_i	Input resistance	1	-	-	MΩ
C_i	Input capacitance	-	-	5	pF
Output levels					
V_{OL}	Low-level output voltage (@ +100 µA)	0	-	0.2	V
V_{OH}	High-level output voltage (@ -100 µA)	V_{DD_IO} - 0.2	-	V_{DD_IO}	V
T_r/T_f	Rise and fall time that can be present on outputs at Cload = 20 pF max	-	-	10	ns

Table 7. Pull-up and pull-down characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
R_{PU}	Equivalent pull-up resistance	V_{DD_IO} = 0 V	-	50	-	kΩ
R_{PD}	Equivalent pull-down resistance	V_{DD_IO} = 1.8 V	-	50	-	kΩ

Table 8. IOL and IOH characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
I_{OL}	Sink current	V_{OL} = Max	X[1]	-	-	mA
I_{OH}	Source current	V_{OH} = Min	X[1]	-	-	mA

1. X can be 2, 4, or 8 depending on the type of the I/O (X denotes the drive strength of output stage).

Note: If the V_{DD_IO} supply is powered down, external activity on the IOs is not allowed.

13.4. Current Consumption

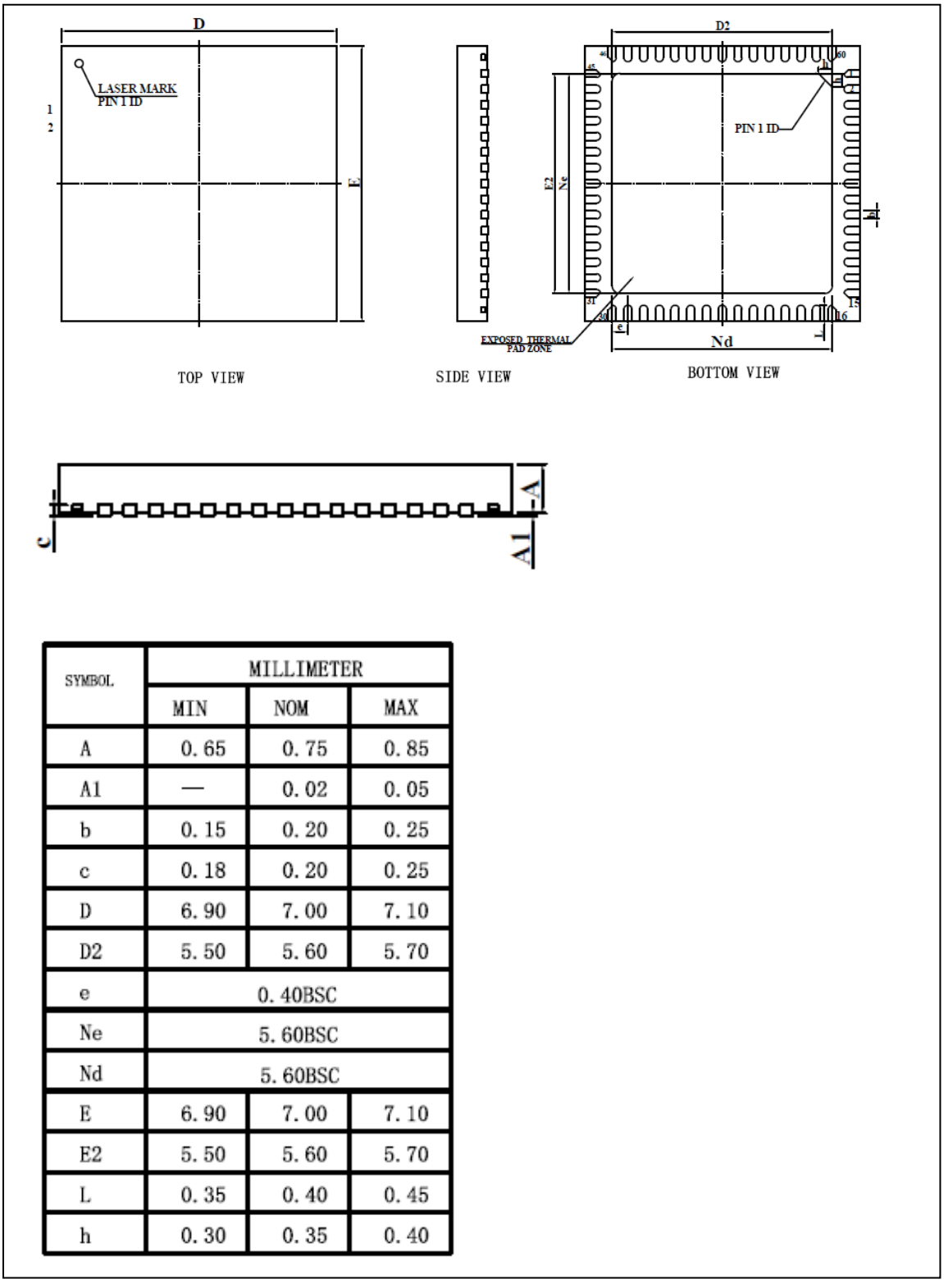
All I/Os, except analog I/Os or otherwise specified are standard I/Os with levels complying with the EIA/JEDEC standard JESD8-7.

Table 9. Current

Core Current	HCLK Run While（1）	@1.8V Not use Codec	@2.5V	@3.3V	Unit
	26MHz	5.5	6.7	7	mA
	100MHz	14.2	20.6	21	mA
	200MHz	24.1	36.9	38.6	mA
I/O current	HCLK Run While（1）	@1.8V	@2.5V		mA
	26MHz	2.1	4.1		mA
	100MHz	2	3.9		mA
	200MHz	2.6	4.7		mA

14.Package mechanical data

Figure 3. QFN60-60-lead, 7X7mm, 0.4mm pitch, quad flat non-leaded package outline



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.65	0.75	0.85
A1	—	0.02	0.05
b	0.15	0.20	0.25
c	0.18	0.20	0.25
D	6.90	7.00	7.10
D2	5.50	5.60	5.70
e	0.40BSC		
Ne	5.60BSC		
Nd	5.60BSC		
E	6.90	7.00	7.10
E2	5.50	5.60	5.70
L	0.35	0.40	0.45
h	0.30	0.35	0.40

Revision history

Date	Revision	Description
8/21/2018	1.0	Preliminary version
3/18/2019	2.0	Add QFN60 package information
4/26/2019	2.1	Add features for SPI, I^2S, and CODEC
6/11/2019	2.2	Add peripheral I/O register details
6/18/2019	2.3	Update block diagram
9/16/2019	2.4	Update QFN60 pin details