ACH1180 Audio Host Processor

Features

- 64-pin lead-free/RoHS compliant
- QFN or BGA package
- ARM Cortex-M4 with floating point processing option
- Two programmable fractional-N synthesizers to reduce interference
  - Supplies CPU clock frequencies, up to max 200MHz
  - Supplies integrated audio codec
- 960k byte internal SRAM
- SPI serial flash interface
- Support sleep and deep sleep mode for low power consumption
- Integrated high-fidelity stereo audio codec
  - Supports Line-in/out and mic-in/headset out
  - Differential mic input
  - 96dB SNR audio output
  - Optional digital interface (I^2S)
- Multiple external interfaces to adapt to various IoT and applications needs
  - 2 x UART
  - I^2C
  - 2 x low-speed, 10-bit ADCs
  - SPI
  - 11 x GPIO
- Clocks
  - Reference clock input 26MHz
  - Low power clock input at 32.768 kHz
  - 2 x clock outputs
- Timers
  - 8 x 32-bit high speed timers
  - 4 timers with independent interrupts

Description

The ACH1180 is a single-chip host processor solution that is fully optimized for Audio and IoT applications. Built with ARM Cortex-M4, floating point, this host processor runs up to 200MHz (250 DMIPS), and is ideal for audio and video processing. It integrates 960K bytes of embedded SRAM for code and data execution. It also integrates a high-fidelity, 96dB SNR stereo audio codec for audio applications, with two fractional-N synthesizers to provide separate clock frequencies to CPU and audio codec to reduce audio interference. Equipped with various external interfaces, ACH1180 can be design in numerous types of host application scenarios. The ACH1180 also supports a crystal driver interface, thus able to generate reference clock to various wireless connectivity radio controllers, such as Wifi/Bluetooth/Zigbee.

With BGA and QFN package, it supports a high level of integration, compact and cost-effective designs, and delivers fast time-to-market.

Contents

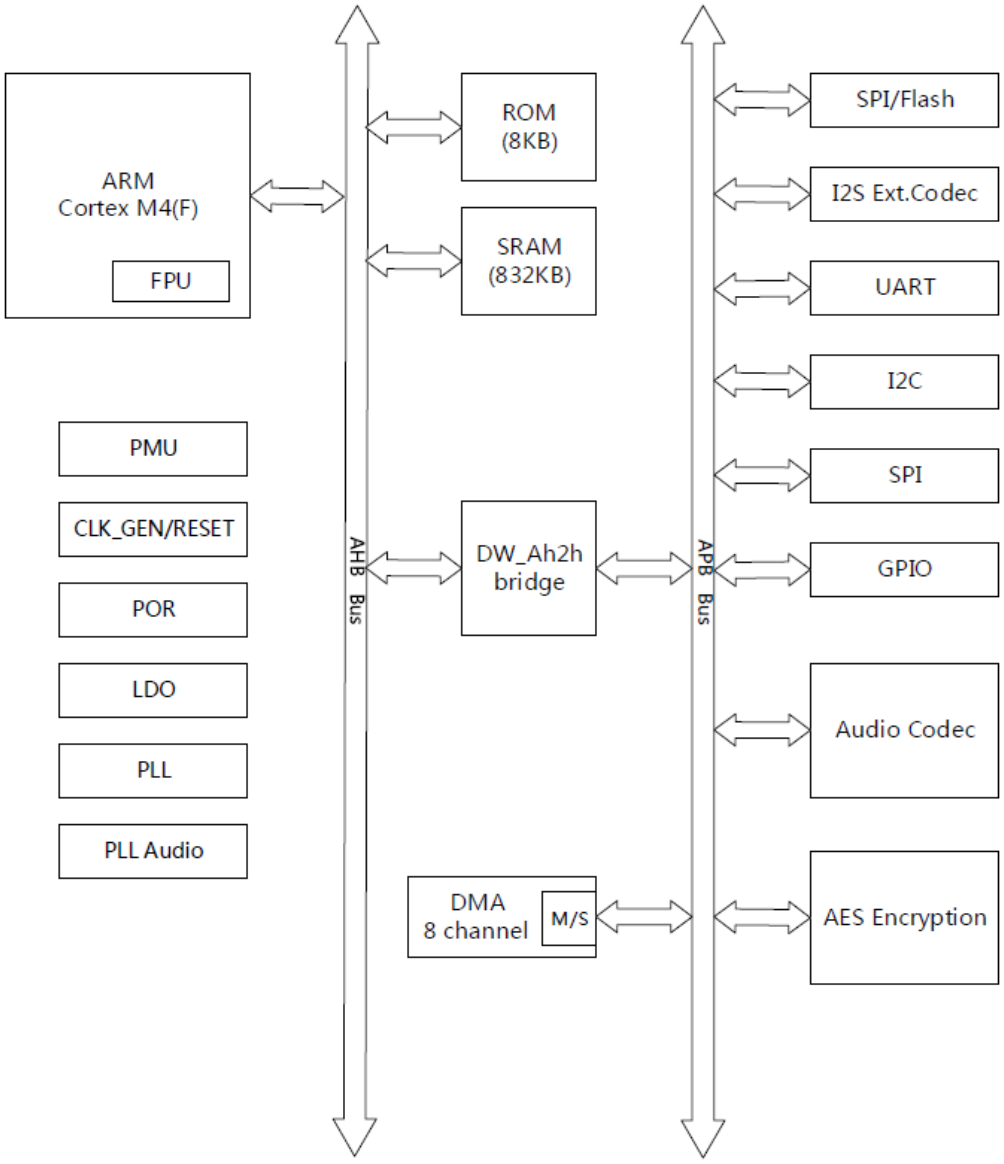
1. Introduction

The ACH1180 is a host processor single-chip solution, fully optimized for audio DSP and wireless host embedded applications featuring an ARM Cortex-M4 floating point processor. Integrating a high-fidelity stereo audio codec, it can support differential microphone inputs, headphone output, and Line-in/out. It also includes two fractional-N PLL blocks providing different high accuracy clocks, for the main CPU and audio codec – significantly reducing interference. The main CPU system can run up to 200MHz for intensive audio/video applications, audio DSP processing, and general purpose application hosting. The ACH1180 also comes with 832K byte internal run-time SRAM. With a variety of external interfaces, UART, SPI, I^2C, I^2S, ADCs, and GPIOs, it can be easily support designs for most applications with lower BOM and external component cost.

2. General Hardware Description

2.1. Block Diagram

Figure 1. ACH1180 detail internal block diagram



2.2. Pin functions

Table 1. ACH1180 functional and supply pin list QFN package

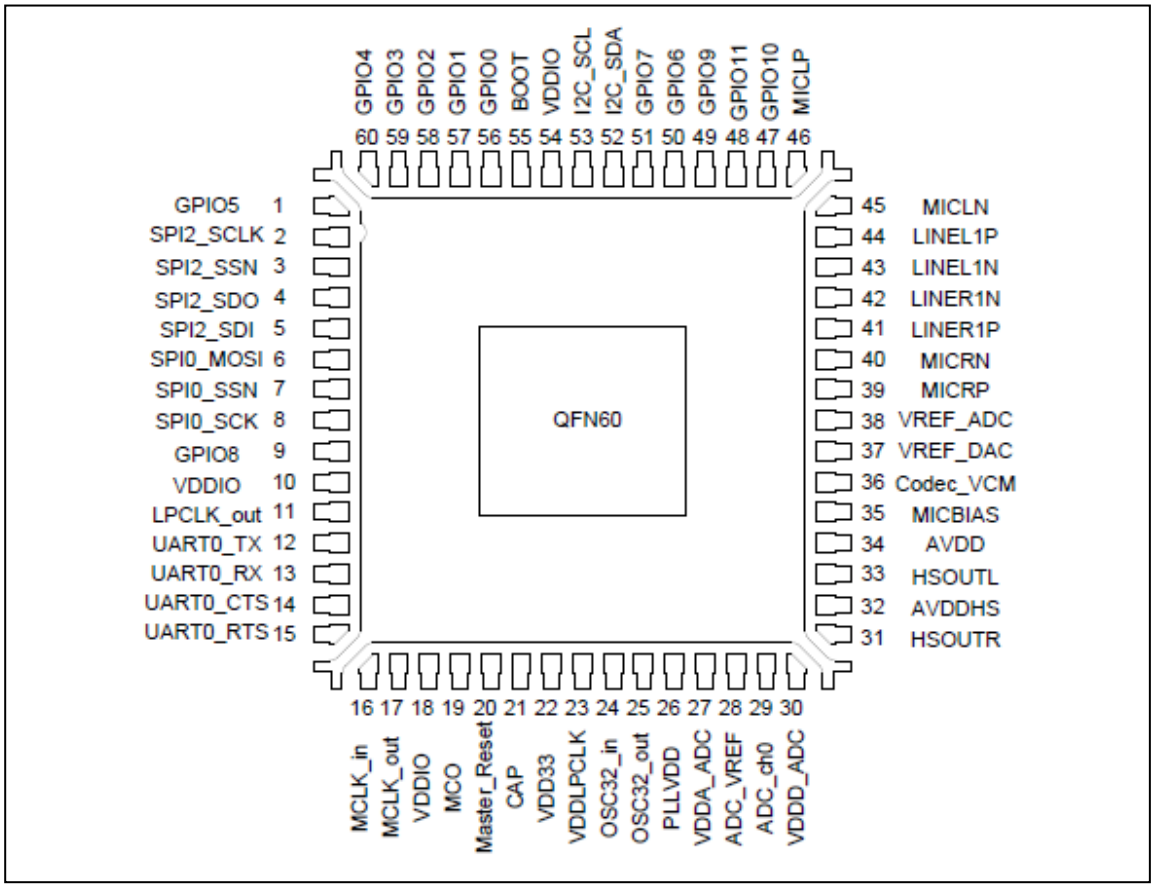
Name (Default)	Alternate usage ALT_0	Alternate usage ALT_1	Description
Digital Signal			
SPI0_MOSI	UART1_CTS		RF Controller Interface
SPI0_NSS	UART1_RTS		
SPI0_SCK	UART1_TX		
SPI0_MISO	UART1_RX	GPIO_8	
UART0_TX			UART0
UART0_RX			
UART0_CTS			
UART0_RTS			
JTDI	UART2_RX	GPIO_10	JTAG
JTDO	UART2_TX	GPIO_11	
TRSTn	UART2_CTS	GPIO_9	
GPIO_0	UART2_RTS		
GPIO_1	I2S1_WS	SPI1_CS	GPIO
GPIO_2	I2S1_CK	SPI1_CLK	
GPIO_3	I2S1_RX	SPI1_MISO	
GPIO_4	I2S1_TX	SPI1_MOSI	
GPIO_5			
SPI2 SCK			SPI2 Serial NOR Flash
SPI2 SS			
SPI2 SDO			
SPI2 SDI			
TCK/SWCLK	GPIO_6		JTAG or User Interface
TMS/SWDIO	GPIO_7		
I2C0_SDA			I2C0
I2C0_SCL			
Clock Signal			
OSC32_IN			32kHz crystal input
OSC32_OUT			32kHz crystal input (differential pair)
OSC_IN			26MHz crystal input
OSC_OUT			26MHz crystal input (differential pair)
MCLK			Audio PLL Clock output
MCO			Main PLL Clock output
CLK32K_OUT			32kHz buffer clock output
Audio Signal			
MICIP_L			Microphone Input
MICIN_L			

MICIP_R			
MICIN_R			
VIP_L			Line-In
VIN_L			
VIP_R			
VIN_R			
ROUT			Line-Out
LOUT			
RHPOUT			Headset Output (8 ohms)
LHPOUT			
Control Signal			
RESET			Reset (Active Low)
BOOT			Test pin
Analog Signal			
ADC0			10-bit ADC
ADC1			10-bit ADC
Reference Signal			
Vcap			
Vref			
MICBIAS			Mic Bias

Name (Default)	Alternate usage ALT_0	Alternate usage ALT_1	Description
Power Supply			
VCCA_PLL1			PLL1 power and ground
GNDA_PLL1			
VCC_HP			CODEC and Headphone power and ground
GND_HP			
VCCA_PLL0			PLL0 and ADC power and ground
GNDA_PLL0			
VDD_CORE_IO			VDD
VDD_CORE_IO			
VDD_CORE_IO			
VSS_CORE_IO			GND
VSS_CORE_IO			
VSS_CORE_IO			

2.3. Pinout Diagram

Figure 2. ACH1180 QFN60 pinout



3. Reset

3.1. Boot modes

An embedded BOOT ROM will run at startup.

When the BOOT PIN is low (0), the SPI 2 is used to load an 8K byte section of an external Flash memory into the internal RAM: loads 8K bytes from location 0x00000000 external Flash to location 0x20000000 internal RAM.

When the BOOT PIN is high (1), the UART 0 boot mode interface will become active. This interface allows data to be loaded from UART 0 into RAM using a set of boot commands. Note that these boot commands are generally used for testing and are not included in this document.

4. Serial Peripheral Interface, SPI

Three SPI ports are supported, usable in Master mode up to 40Mbps. Below is the feature list for the SPI devices:

- Data bus widths of 8, 16, and 32 bits.
- FIFO depth – Configurable depth of the transmit and receive FIFO buffers from 2 to 22 words deep. (note: the final ACH version will support from 2 to 128 word FIFO depth)
- Programmable levels of FIFO interrupt for receive and transmit.
- Independent masking of interrupts – Master collision, transmit FIFO overflow, transmit FIFO empty, receive FIFO full, receive FIFO underflow, and receive FIFO overflow interrupts can all be masked independently.
- Multi-master contention detection – Informs the processor of multiple serial-master accesses on the serial bus.
- Programmable delay on the sample time of the received serial data bit (rxd), when configured in Master Mode; enables programmable control of routing delays resulting in higher serial data-bit rates.
- Serial interface operation – Choice of Motorola SPI, Texas Instruments Synchronous Serial Protocol or National Semiconductor Microwire.
- Clock bit-rate – Dynamic control of the serial bit rate of the data transfer.
- Number of slave select outputs –1 to 16 serial slave-select output signals can be generated.
- Hardware/software slave-select – Dedicated hardware slave-select lines can be used or software control can be used to target the serial-slave device.
- Interrupt polarity – This configuration option selects the active level of the output interrupt lines.
- Serial clock polarity – This configuration option selects the serial-clock polarity of the SPI format directly after reset.
- Serial clock phase – This configuration option selects the serial-clock phase of the SPI format directly after reset.

5. Inter-integrated Sound, I²S

Two I²S ports supporting Master mode are available. One of these ports is routed to the internal integrated CODEC, and is not connectable to external pins. The other I²S port is for external peripheral access. Below are the features:

- I2S transmitter and/or receiver based on the Philips I²S serial protocol.
- Configurable number of stereo channels (up to 4) for both transmitter and receiver.
- Full duplex communication due to the independence of transmitter and receiver.
- Asynchronous clocking of APB bus and I2S sclk.
- Master mode of operation.
- Audio data resolutions of 12, 16, 20, 24, and 32 bits per sample.
- FIFO depth of 16 samples.
- Programmable FIFO thresholds.

6. Audio CODEC

An integrated audio CODEC is available in the ACH. Control registers are mapped to the APB bus. Audio data is sent using a dedicated I²S port. The following features are supported:

- 24-bit D/A and A/D conversion.
- 90dB Dynamic Range and -80dB THD A/D Conversion.
- 96dB Dynamic Range and -86dB THD D/A Conversion.
- 2 Stereo Single-Ended/Differential Line-in and Microphones inputs.
- 1 Stereo Single-Ended Headset Driver.
- Built-in Microphone Bias.
- Built-in References and Biasing Circuitry.
- Analogue and Digital Gain with Soft-ramp Control.
- Input Automatic Volume Control (ALC).
- Power-on/off Pop-Suppression.
- Supported Audio Sampling Rates from 8 to 192 kHz.
- LPC standard I2S audio data interface in Master and Slave Mode Operation.

7. Clock specifications

The ACH11800 uses two clocks: a reference clock and an optional low power clock. For the reference clock, the ACH1180 can either use an external reference clock source or generate its own reference using a XTAL. The low-power clock must always be supplied from an external source.

Table 2. Main crystal specifications

Symbol	Parameter	Min	Typ	Max	Unit
External crystal					
F_{IN}	Clock input frequency list		26		MHz
F_{INTOL}	Tolerance on input frequency (typical)	-20	-	+20	ppm

Table 3. Low power clock specifications

Symbol	Parameter	Min	Typ	Max	Unit
F_{IN}	Clock input frequencies		32.768		kHz
F_{INTOL}	Tolerance on input frequency	-1000	-	+1000	ppm

8. Electrical Characteristics

8.1. Absolute maximum ratings

The Absolute Maximum Rating (AMR) corresponds to the maximum value that can be applied without leading to instantaneous or very short-term unrecoverable hard failure (destructive breakdown).

Table 4. Absolute maximum ratings

Symbol	Parameter	Min	Max	Unit
V_{DD}	Digital Supply voltages	-0.3	+3.3	V
V_{CCA_PLL}	Analog PLL Supply voltage	-0.3	+3.6	V
V_{CC_HP}	Supply voltage I/O	-0.3	+3.6	V
$V_{CCA\_MAIN\_PLL}$	Supply voltage I/O	-0.3	+3.6	V
V_{in}	Input voltage on any digital pin	-0.3	+3.3	V
V_{ssdiff}	Maximum voltage difference between different types of Vss pins	-0.3	+0.3	V
T_{stg}	Storage temperature	-65	+100	°C

8.2. Operating ranges

Operating ranges define the limits for functional operation and parametric characteristics of the device. Functionality outside these limits is not guaranteed.

Table 5. Operating ranges

Symbol	Parameter	Min	Typ	Max	Unit
T_{amb}	Operating ambient temperature	-30	+25	+70	°C
V_{DD}	Digital Supply Voltage	+1.8	+2.5	+3.3	V
V_{CCA_PLL}	Analog Audio PLL Supply Voltage	+1.8	+2.5	+3.6	V
V_{CC_HP}	Analog Headset Supply Voltage	+2.5	+3.3	+3.6	V
$V_{CCA\_MAIN\_PLL}$	Analog Main PLL Supply Voltage	+1.8	+3.3	+3.6	V

8.3. Digital I/O specifications

All I/Os, except analog I/Os or otherwise specified are standard I/Os with levels complying with the EIA/JEDEC standard JESD8-7.

Table 6. DC and AC input specifications

Symbol	Parameter	Min	Typ	Max	Unit
Input levels					
V_{IL}	Low-level input voltage	0	-	0.35 * V_{DD_IO}	V
V_{IH}	High-level input voltage	0.65 * V_{DD_IO}	-	-	V
V_{hyst}	Schmitt trigger hysteresis	150	-	-	mV
T_r/T_f	Rise and fall time that can be present on inputs	-	-	25	ns
R_i	Input resistance	1	-	-	MΩ
C_i	Input capacitance	-	-	5	pF

Output levels					
V_{OL}	Low-level output voltage (@ +100 µA)	0	-	0.2	V
V_{OH}	High-level output voltage (@ -100 µA)	V_{DD_IO} - 0.2	-	V_{DD_IO}	V
T_r/T_f	Rise and fall time that can be present on outputs at Cload = 20 pF max	-	-	10	ns

Table 7. Pull-up and pull-down characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Unit
R_{PU}	Equivalent pull-up resistance	V_{DD_IO} = 0 V	-	50	-	kΩ
R_{PD}	Equivalent pull-down resistance	V_{DD_IO} = 1.8 V	-	50	-	kΩ

Table 8. IOL and IOH characteristics

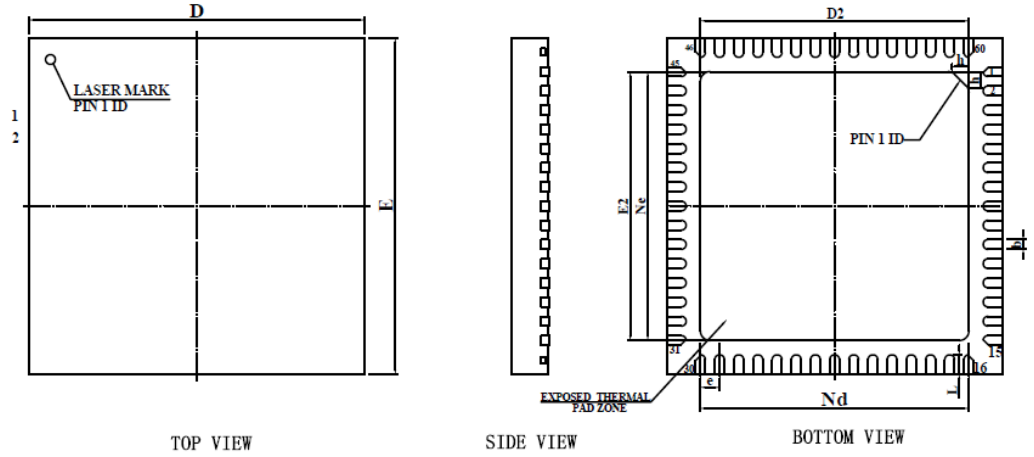
Symbol	Parameter	Condition	Min	Typ	Max	Unit
I_{OL}	Sink current	V_{OL} = Max	X[1]	-	-	mA
I_{OH}	Source current	V_{OH} = Min	X[1]	-	-	mA

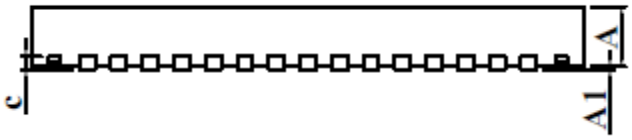
1. X can be 2, 4, or 8 depending on the type of the I/O (X denotes the drive strength of output stage).

Note: If the V_{DD_IO} supply is powered down, external activity on the IOs is not allowed.

9. Package mechanical data

Figure 3. QFN60-60-lead, 7X7mm, 0.4mm pitch, quad flat non-leaded package outline





SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.65	0.75	0.85
A1	—	0.02	0.05
b	0.15	0.20	0.25
c	0.18	0.20	0.25
D	6.90	7.00	7.10
D2	5.50	5.60	5.70
e	0.40BSC		
Ne	5.60BSC		
Nd	5.60BSC		
E	6.90	7.00	7.10
E2	5.50	5.60	5.70
L	0.35	0.40	0.45

Revision history

Date	Revision	Description
8/21/2018	1.0	Preliminary version
3/18/2019	2.0	Add QFN60 package information
4/26/2019	2.1	Add features for SPI, I^2S, and CODEC